UTM
UNIVERSITI TEKNOLOGI MALAYSIA

Sekolah Pendidikan Profesional dan
Pendidikan Berterusan
(SPACE)

FINAL EXAMINATION / *PEPERIKSAAN AKHIR*
SEMESTER 1 – SESSION 2019 / 2020
PROGRAM KERJASAMA

COURSE CODE *KOD KURSUS*	:	DDWE 1123
COURSE NAME *NAMA KURSUS*	:	DIGITAL ELECTRONICS *ELEKTRONIK DIGITAL*
YEAR / PROGRAMME *TAHUN / PROGRAM*	:	1 DDWE/B/K
DURATION *TEMPOH*	:	2 HOURS 30 MINUTES / *2 JAM 30 MINIT*
DATE *TARIKH*	:	NOV 2019

INSTRUCTION/*ARAHAN* :

1. ANSWER ALL QUESTIONS.
   JAWAB SEMUA SOALAN .

2. DETACH **PAGE 13** AND ATTACH TO YOUR ANSWER BOOKLETS.
   *CERAIKAN **MUKASURAT 13** DAN LAMPIRKAN PADA BUKU JAWAPAN ANDA.*

(You are required to write your name and your lecturer's name on your answer script)
(Pelajar dikehendaki tuliskan nama dan nama pensyarah pada skrip jawapan)

STUDENT'S NAME / *NAMA PELAJAR*	:	.....
I.C NO. / *NO. K/PENGENALAN*	:	.....
YEAR / PROGRAMME *TAHUN / PROGRAM*	:	.....
COLLEGE NAME *NAMA KOLEJ*	:	.....
LECTURER'S NAME *NAMA PENSYARAH*	:	.....

This examination paper consists of **13** pages including the cover
*Kertas soalan ini mengandungi **13** muka surat termasuk kulit hadapan*

PETIKAN DARIPADA PERATURAN AKADEMIK
ARAHAN AM - PENYELEWENGAN AKADEMIK

1. SALAH LAKU SEMASA PEPERIKSAAN

1.1 Pelajar tidak boleh melakukan mana-mana salah laku peperiksaan seperti berikut :-

1.1.1 memberi dan/atau menerima dan/atau memiliki sebarang maklumat dalam bentuk elektronik, bercetak atau apa jua bentuk lain yang tidak dibenarkan semasa berlangsungnya peperiksaan sama ada di dalam atau di luar Dewan Peperiksaan melainkan dengan kebenaran Ketua Pengawas; atau

1.1.2 menggunakan makluman yang diperolehi seperti di atas bagi tujuan menjawab soalan peperiksaan; atau

1.1.3 menipu atau cuba untuk menipu atau berkelakuan mengikut cara yang boleh ditafsirkan sebagai menipu semasa berlangsungnya peperiksaan; atau

1.1.4 lain-lain salah laku yang ditetapkan oleh Universiti (seperti membuat bising, mengganggu pelajar lain, mengganggu Pengawas menjalankan tugasnya).

2. HUKUMAN SALAH LAKU PEPERIKSAAN

2.1 Sekiranya pelajar didapati telah melakukan pelanggaran mana-mana peraturan peperiksaan ini, setelah diperakukan oleh Jawatankuasa Peperiksaan Fakulti dan disabitkan kesalahannya, Senat boleh mengambil tindakan dari mana-mana satu yang berikut :-

2.1.1 memberi markah SIFAR (0) bagi keseluruhan keputusan peperiksaan kursus yang berkenaan (termasuk kerja kursus); atau

2.1.2 memberi markah SIFAR (0) bagi semua kursus yang didaftarkan pada semester tersebut.

2.2 Jawatankuasa Akademik Fakulti boleh mencadangkan untuk diambil tindakan tatatertib mengikut peruntukan Akta Universiti dan Kolej Universiti, 1971, Kaedah-kaedah Universiti Teknologi Malaysia (Tatatertib Pelajar-pelajar), 1999 bergantung kepada tahap kesalahan yang dilakukan oleh pelajar.

2.3 Pelajar yang didapati melakukan kesalahan kali kedua akan diambil tindakan seperti di perkara 2.1.2 dan dicadang untuk diambil tindakan tatatertib mengikut peruntukan Akta Universiti dan Kolej Universiti, 1971, Kaedah-kaedah Universiti Teknologi Malaysia (Tatatertib Pelajar-pelajar), 1999.

Q1. (a) (i) With an aid of diagram, define digital quantities.
Dengan bantuan gambar rajah, definisikan kuantiti digital.

(ii) One of the advantages of digital techniques are easier to design, explain briefly.
Salah satu kelebihan teknik digital adalah lebih mudah untuk direkabentuk, terangkan secara ringkas

(4 marks/*markah*)

(b) Convert the following numbers as indicated:
Tukar nombor berikut seperti yang ditunjukkan :

(i) 225.225_{10} to binary, octal and hexadecimal.
225.225_{10} kepada binari, perlapanan dan perenambelasan

(ii) 11010111.110_2 to octal .
11010111.110_2 kepada perlapanan

(8 marks/*markah*)

(c) Most calculator use BCD to store the decimal values as they are entered into the keyboard and to drive the digit displays.
Kebanyakan kalkulator menggunakan BCD untuk menyimpan nilai perpuluhan apabila ia dimasukkan ke dalam papan kekunci dan untuk memacu digit yang dipaparkan.

(i) If a calculator is designed to handle 8-digit decimal numbers, how many bits does this require?
Jika kalkulator direka untuk mengendalikan nombor perpuluhan 8 digit, berapa banyak bit yang diperlukan?

(ii) What bits are stored when the number 180 is entered into the calculator?
Apakah bit yang disimpan apabila nombor 180 dimasukkan ke dalam kalkulator?

(4 marks/markah)

(d) Perform arithmatic process for -17 - (-17) by using 1's complement system. Use eight bits (including sign bit) for each number and convert the binary result back to decimal.
Laksanakan proses aritmatik bagi -17 – (-17) dengan menggunakan sistem pelengkap 1. Gunakan lapan bit (termasuk bit tanda) untuk setiap nombor dan tukarkan hasil perduaan kembali ke perpuluhan.

(5 marks/*markah*)

(e) Convert 274_{10} and 126_{10} to BCD and then perform BCD addition. Convert your result back to decimal.

Tukarkan 274_{10} dan 126_{10} kepada BCD dan kemudian laksanakan hasiltambah BCD. Tukar hasil anda kembali ke perpuluhan.

(5 marks/*markah*)

Q2. (a) Figure Q2(a) shows a logic circuit diagram for a particular digital system that operated when the output F is active-LOW. By employing alternative logic gates, draw the equivalent logic circuit representation to determine the possible input combinations to operate the digital system.

Rajah Q2(a) menunjukkan sebuah gambar rajah litar logik bagi satu sistem digital yang beroperasi apabila keluaran F adalah aktif-RENDAH. Dengan mengunakan get-get logik alternatif, lukiskan perwakilan litar logik yang setara untuk menentukan kombinasi-kombinasi masukan yang berkemungkinan untuk membolehkan sistem digital tersebut beroperasi.

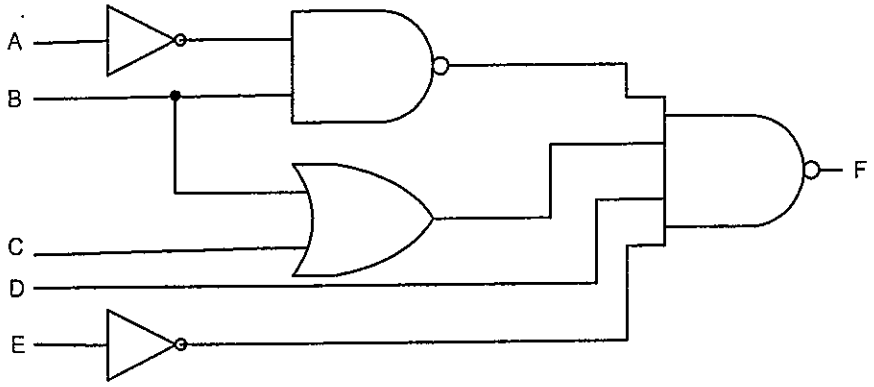


Figure Q2(a) / *Rajah Q2(a)*

(8 marks/*markah*)

(b) Draw the simplest possible logic diagram that implements the output Y of the logic diagram in Figure Q2(b) by using Boolean Algebra and deMorgan theorem if necessary.

Lukis gambarajah logik paling mudah yang boleh melaksanakan keluaran Y dalam gambar rajah logik yang diberikan di Rajah Q2(b) dengan menggunakan Aljabar Boolean dan teorem deMorgan jika perlu.

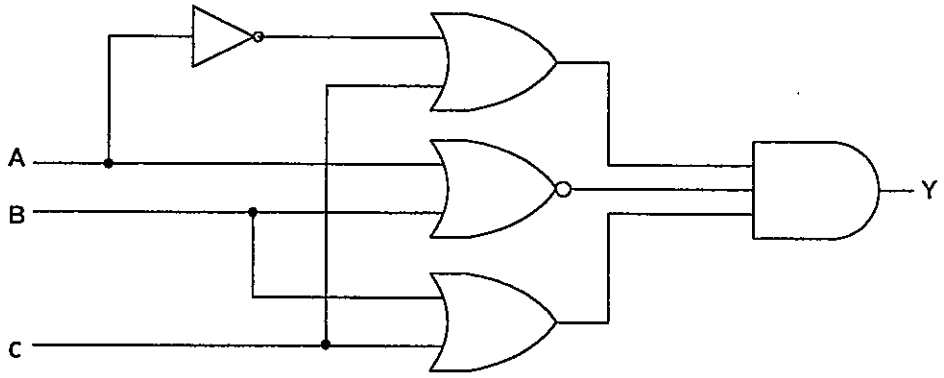


Figure Q2(b) / *Rajah Q2(b)*

(6 marks/*markah*)

Q3. Figure Q3 (a) shows a diagram for an automobile alarm circuit used to detect certain undesirable conditions. The three switches, S2, S1 and S0 are used to indicate the status of the door by the driver's seat, the ignition and the headlights, respectively. Design the logic circuit with these three switches as inputs so that the alarm will be activated whenever either of the following conditions exists:

- The headlights are ON while the ignition is OFF.
- The door is open while the ignition is on.

Rajah Q3 (a) menunjukkan gambar rajah bagi litar penggera automobil yang digunakan untuk mengesan keadaan tertentu yang tidak diingini Tiga suis, S2, S1 dan S0 digunakan untuk menunjukkan status pintu oleh kerusi pemandu, pencucuhan dan lampu hadapan. Reka bentuk litar logik dengan tiga suis ini sebagai masukan supaya penggera akan diaktifkan apabila salah satu daripada keadaan berikut wujud:

- *Lampu hadapan adalah HIDUP semasa pencucuhan diMATIkan.*
- *Pintu terbuka semasa pencucuhan diHIDUPkan.*

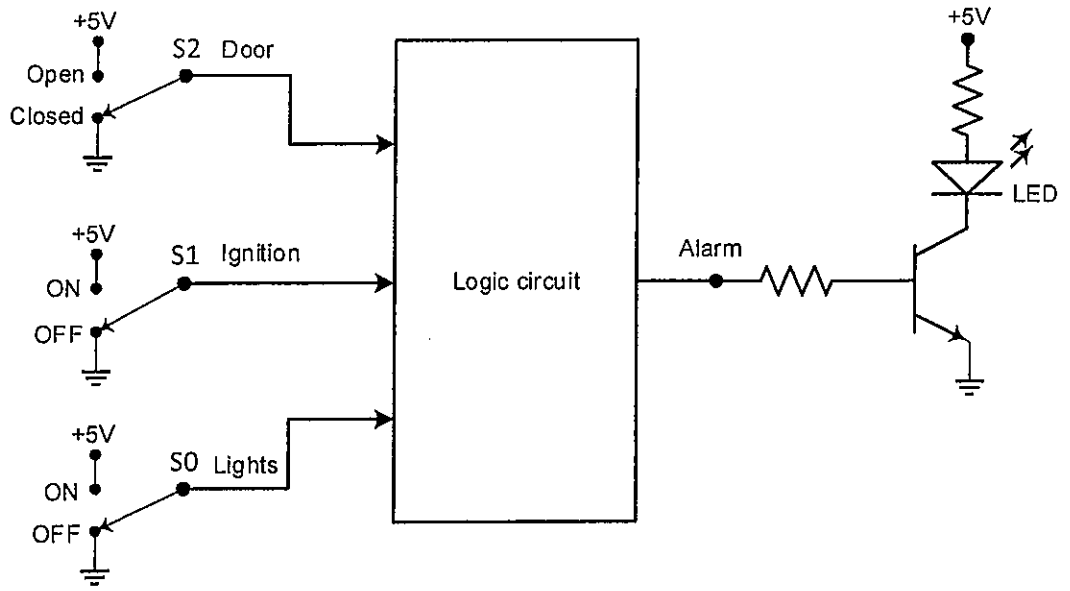


Figure Q3(a) / *Rajah Q3 (a)*

(15 marks/*markah*)

(b) Consider the following circuit in Figure Q3(b) with an active HIGH output decoder. Construct a truth table for X and Y in terms of A, B and C.
Pertimbangkan litar berikut dalam Rajah Q3(b) dengan keluaran penyahkod yang aktif. TINGGI. Hasilkan jadual kebenaran untuk X dan Y dalam terma A, B dan C.

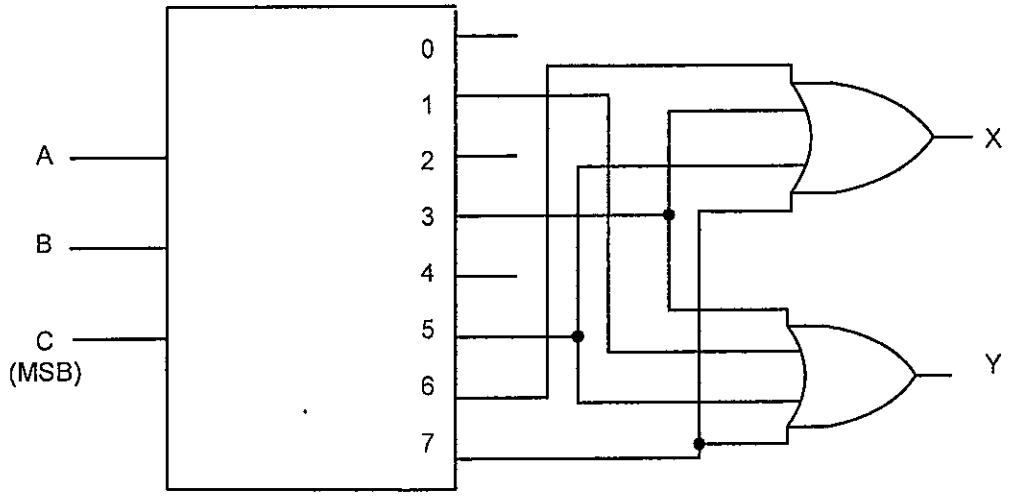


Figure Q3(b) / *Rajah Q3(b)*

(8 marks/*markah*)

Q4. (a) State two(2) drawback caused by propagation delays in asynchronous counters.
Nyatakan dua(2) kelemahan yang disebabkan oleh lengah perambatan dalam pembilang tak segerak.

(2 marks/*markah*)

(b) Refer Figure Q4(b)(i), sketch the output waveform of Q1 and Q2 in Figure Q4(b)(ii) in an attachment sheet based on the given timing diagram;

i. output Q1 when there is no CLR input,

ii. output Q2 when the CLR input is as shown.

Assume the initial condition of Q is LOW.

Rujuk Rajah Q4(b)(i), lakarkan gelombang keluaran bagi Q1 dan Q2 dalam Rajah Q4(b)(ii) di dalam helaian lampiran berdasarkan gambar rajah pemasaan yang diberi;

i. keluaran Q1 apabila tiada masukan CLR,

ii. keluaran Q2 apabila masukan CLR adalah seperti yang ditunjukkan.

Anggap keadaan awal bagi Q adalah RENDAH.

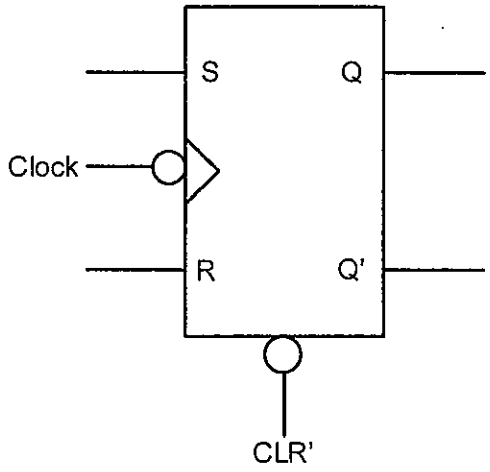


Figure Q4(b)(i) / *Rajah Q4(b)(i)*

(8 marks/*markah*)

(c) Figure Q4(c) is a bidirectional register 74194;
Rajah Q4(c) adalah sebuah pendaftar dwihala 74194;

i. Why it is called as universal bidirectional shift register?
Mengapa ia dinamakan sebagai pendaftar dwihala universal?

ii. Is the CLR input synchronous or asynchronous?
Adakah masukan CLR segerak atau tak segerak?

iii. Assume the following conditions:
Anggap syarat seperti yang berikut:

$Q_A\ Q_B\ Q_C\ Q_D = 1011$

A B C D = 0110

$\overline{CLR} = 1$

SR SER = 0

SL SER = 1

If S0= 1 and S1 =1, what will the register outputs be after one CLK pulse, after two CLK pulses, after three CLK pulse and after four CLK pulse.
Jika S0 = 1 dan S1 = 1, apakah yang keluaran daftar selepas denyutan CLK pertama, selepas denyutan CLK kedua, selepas denyutan CLK ketiga dan selepas denyutan CLK keempat.

iv. Use the same conditions as in part (iii), except assume that output Q_A is connected to SL SER, what will be the register outputs after four CLK pulses?
Menggunakan syarat yang sama seperti dalam bahagian (iii), kecuali mengandaikan bahawa keluaran Q_A adalah disambung kepada SL SER apa keluaran daftar selepas denyutan CLK keempat?.

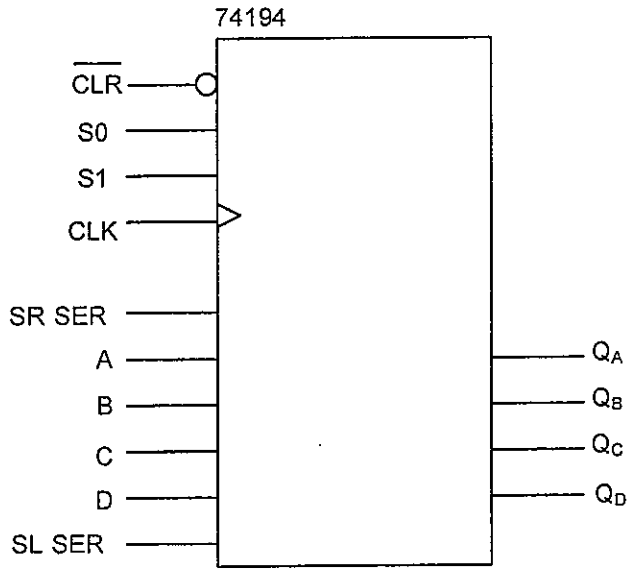


Figure Q4(c) / *Rajah Q4(c)*

(9 marks/*markah*)

Q5. (a) A certain logic family has the following voltage parameters:
Sesetengah keluarga logik mempunyai parameter voltan berikut

V_{IH} (min) = 3.5V V_{IL} (max) = 1.0V
V_{OH} (min)= 4.9V V_{OL} (max)=0.1V

(i) what is the largest positive going noise spike that can be tolerated?
apakah hingar ke positif terbesar yang boleh diterima?

(ii) what is the largest negative going noise spike that can be tolerated?
apakah hingar ke negatif terbesar yang boleh diterima?

(4 marks/*markah*)

(b) (i) Define propagation delays and describe two(2) types of propagation delay.
Definisikan lengah perambatan dan jelaskan dua(2) jenis lengah perambatan.

(ii) Calculate the power dissipation for 74S and 74LS series for the given datasheet in attachment sheet where V_{CC} = 5.5 V.
Kirakan pelesapan kuasa bagi siri 74S dan 74LS untuk lampiran data yang diberi dalam helaian lampiran di mana V_{CC} = 5.5 V

(9 marks/*markah*)

(c) (i) Draw an IEEE/ANSI notation for open-collector and open-drain outputs.
Lukiskan notasi IEEE/ANSI untuk pemungut-buka dan keluaran saliran-buka.

(ii) Why do open-collector outputs need a pull-up resistor?
Mengapakah keluaran pemungut-buka memerlukan perintang tarik-naik?

(5 marks/*markah*)

SDLS075

SN54194, SN54LS194A, SN54S194, SN74194, SN74LS194A, SN74S194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

MARCH 1974—REVISED MARCH 1988

- Parallel Inputs and Outputs
- Four Operating Modes:
  - Synchronous Parallel Load
  - Right Shift
  - Left Shift
  - Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overriding Clear

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'194	36 MHz	195 mW
'LS194A	36 MHz	75 mW
'S194	105 MHz	425 mW

description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

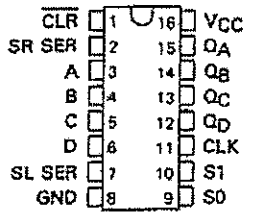
- Inhibit clock (do nothing)
- Shift right (in the direction Q_A toward Q_D)
- Shift left (in the direction Q_D toward Q_A)
- Parallel (broadside) load

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

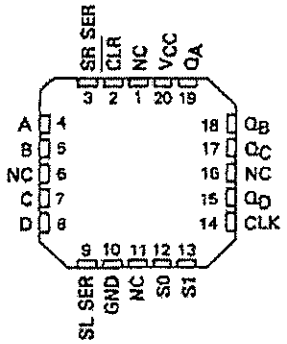
Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the shift register is inhibited when both mode control inputs are low. The mode controls of the SN54194/SN74194 should be changed only while the clock input is high.

SN54194, SN54LS194A, SN54S194 . . . J OR W PACKAGE
SN74194 . . . N PACKAGE
SN74LS194A, SN74S194 . . . D OR N PACKAGE
(TOP VIEW)

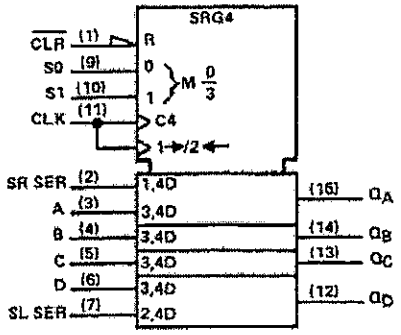


SN54LS194A, SN54S194 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54194, SN54LS194A, SN54S194
SN74194, SN74LS194A, SN74S194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

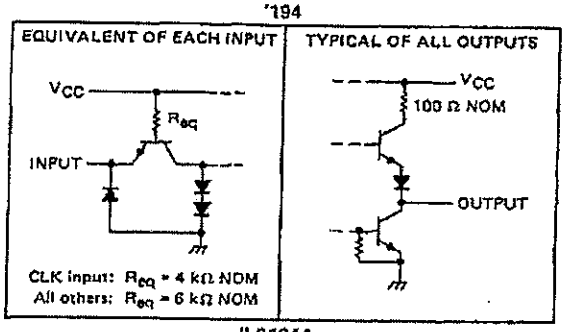
FUNCTION TABLE

INPUTS									OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL						
	S1	S0		LEFT	RIGHT	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

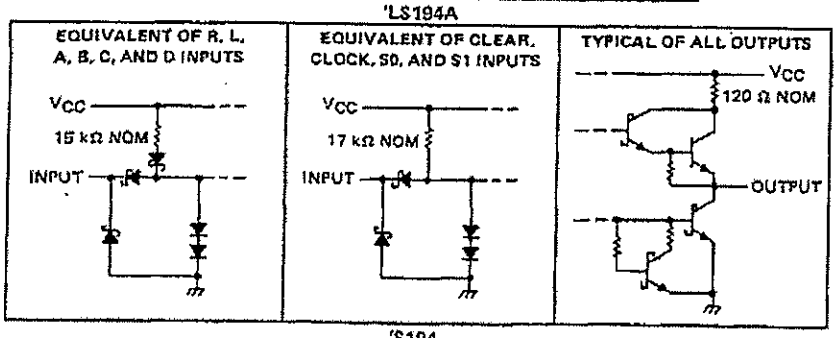
H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

schematics of inputs and outputs

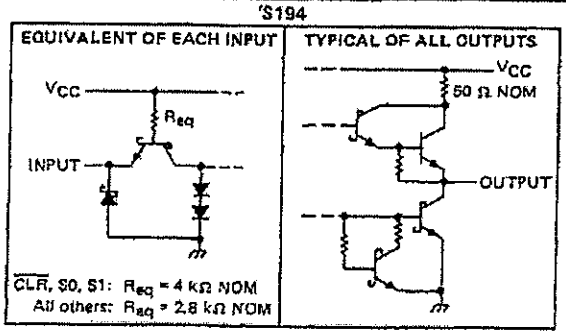
'194



'LS194A



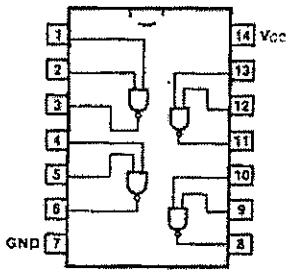
'S194



54/7400 011065
54H/74H00 011069
54S/74S00 011574
54LS/74LS00 011068

QUAD 2-INPUT NAND GATE

CONNECTION DIAGRAMS
PINOUT A

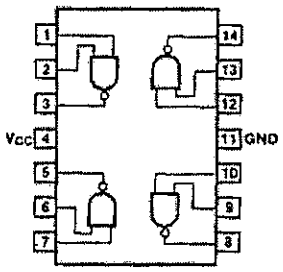


4

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7400PC, 74H00PC 74LS00PC, 74S00PC		9A
Ceramic DIP (D)	A	7400DC, 74H00DC 74LS00DC, 74S00DC	5400DM, 54H00DM 54LS00DM, 54S00DM	6A
Flatpak (F)	A	74LS00FC, 74S00FC	54LS00FM, 54S00FM	3I
	B	7400FC, 74H00FC	5400FM, 54H00FM	

PINOUT B



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply	8.0		16.8			16		1.6	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}	Current	22		40			36		4.4		V_{IN} = Open	
t_{PLH}	Propagation Delay	22		10		2.0	4.5		10	ns	Figs. 3-1, 3-4	
t_{PHL}		15		10		2.0	5.0		10			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

Attachment sheet / *Helaian lampiran*

Name:_____

ID Number:_____

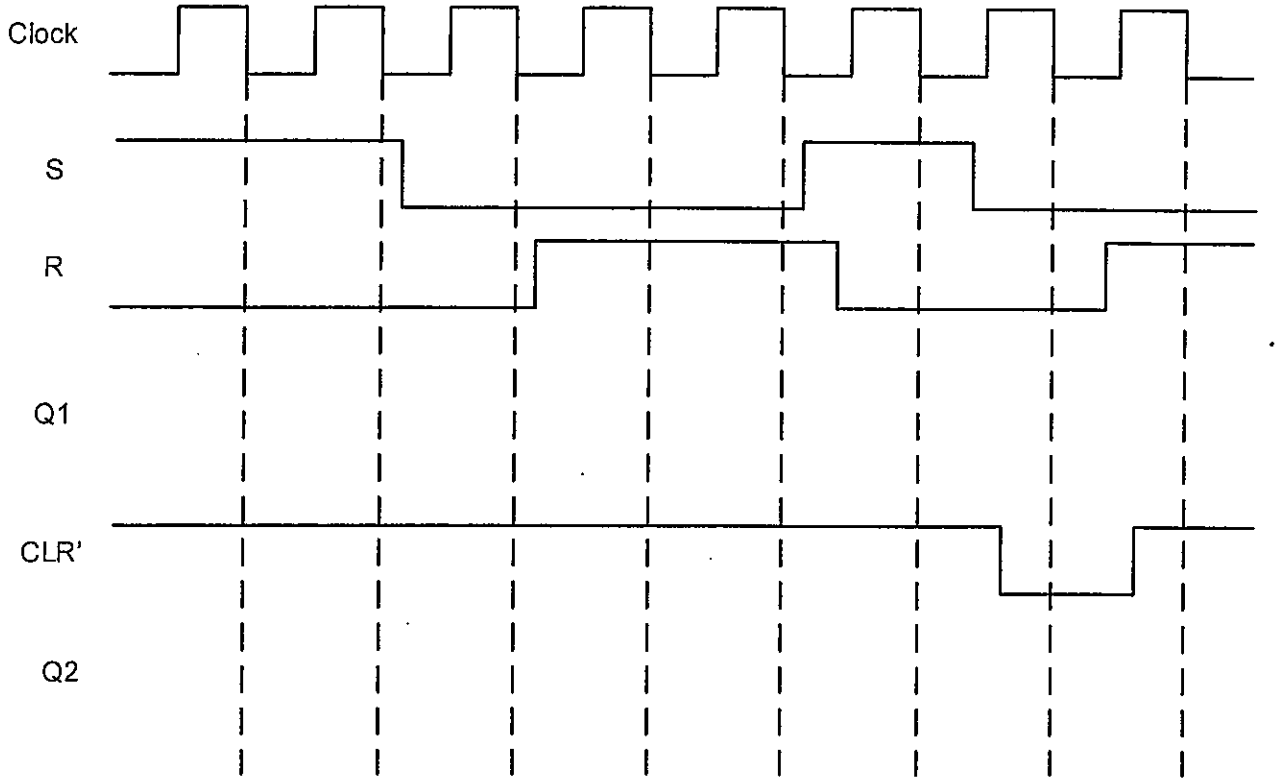


Figure Q4(b) (ii) / *Rajah Q4(b) (ii)*

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