DDPB

UTM UNIVERSITI TEKNOLOGI MALAYSIA

SekolahPendidikanProfesionaldan
PendidikanBerterusan
(UTMSPACE)

FINAL EXAMINATION / *PEPERIKSAAN AKHIR*
SEMESTER 1 – SESSION 2016 / 2017
PROGRAM KERJASAMA

COURSE CODE *KOD KURSUS*	:	DDWE 1123
COURSE NAME *NAMA KURSUS*	:	DIGITAL ELECTRONIC / *ELEKTRONIK DIGITAL*
YEAR / PROGRAMME *TAHUN / PROGRAM*	:	1 DDWE/ K/B
DURATION *TEMPOH*	:	2 HOURS 30 MINUTES / *2 JAM 30 MINIT*
DATE *TARIKH*	:	OCT 2016

INSTRUCTION :
ARAHAN

1. ANSWER ALL QUESTIONS.
   JAWAP SEMUA SOALAN .

2. DETACH **PAGES 13** AND **14** AND ATTACH TO YOUR ANSWER BOOKLETS.
   *CERAIKAN **MUKASURAT 13** DAN **14** DAN LAMPIRKAN PADA BUKU JAWAPAN ANDA.*

(You are required to write your name and your lecturer's name on your answer script)
(Pelajar dikehendaki menulis nama dan nama pensyarah pada skrip jawapan)

NAME / *NAMA PELAJAR*	:	.....
I.C NO. / *NO. K/PENGENALAN*	:	.....
YEAR / COURSE *TAHUN / KURSUS*	:	.....
COLLEGE NAME *NAMA KOLEJ*	:	.....
LECTURER'S NAME *NAMA PENSYARAH*	:	.....

This examination paper consists of ...14... pages including the cover
Kertas soalan ini mengandungi .....14..... muka surat termasuk kulit hadapan

Q1. (a) i. State an advantage and limitation of digital techniques over analog technique.
Nyatakan satu kelebihan dan had bagi teknik digital berbanding teknik analog.

ii. Which of the following are analog quantities and which are digital quantitites?
a. Number of atoms in a sample of material.
b. Pressure in a bicycle tyre.
c. Timer setting on a microwave oven.
Manakah yang berikut adalah kuantiti analog dan yang manakah kuantiti digital?
a. Bilangan atom dalam bahan sampel.
b. Tekanan dalam tayar basikal.
c. Tetapan pemasa di dalam ketuhar gelombang mikro.

(5 marks/*markah*)

(b) Convert the following number/code to decimal number and show your work clearly
Tukarkan nombor / kod berikut kepada nombor desimal dan tunjukkan jalan kerja dengan jelas..
i. 100110000011_{Gray}
ii. 516_8
iii. 10010100_{BCD}

(7 marks/*markah*)

(c) Perform the following operations in 2's complement system. Use 8 bits (including the sign bits) and convert the result back to decimal number.
Laksanakan operasi berikut dalam sistem pelengkap 2. Gunakan 8 bit (termasuk bit tanda) dan tukarkan semula jawapan kepada nombor desimal.
i. $85_{10} - 51_{10}$
ii. $-56_{10} + 23_{10}$

(6 marks/*markah*)

(d) What is the range of unsigned decimal values that can be represented in 10 bits 2's complement? What is the range of signed decimal values using the same number of bits?
Apakah julat nilai desimal tidak bertanda yang boleh diwakilikan dalam 10 bit bagi pelengkap 2? Apakah julat nilai desimal bertanda menggunakan nilai bit yang sama?

(2 marks/*markah*)

Q2. (a) Simplify the following expression using Boolean Algebra and deMorgan theorem.
Ringkaskan persamaan berikut menggunakan Aljabar Boolean dan teorem deMorgan.

i. $P = \overline{(A + \overline{B})}\overline{B} + AB\overline{C} + \overline{\overline{AB}(\overline{\overline{C} + A})}$

ii. $Q = AB + A\overline{(\overline{C} + AB)} + BC\overline{(A + AC)}$

(8 marks/*markah*)

(b) Convert the following SOP (sum-of-product) expression to an equivalent POS (product-of-sum) expression.
Tukarkan penyataan SOP (hasildarab produk) berikut kepada penyataan POS (hasiltambah produk) yang setaraf.

$$Z = \overline{A}\overline{B}\overline{C} + A\overline{B} + A\overline{C}$$

(5 marks/*markah*)

(c) Refer Figure Q2(c);
Rujuk Rajah Q2(c);

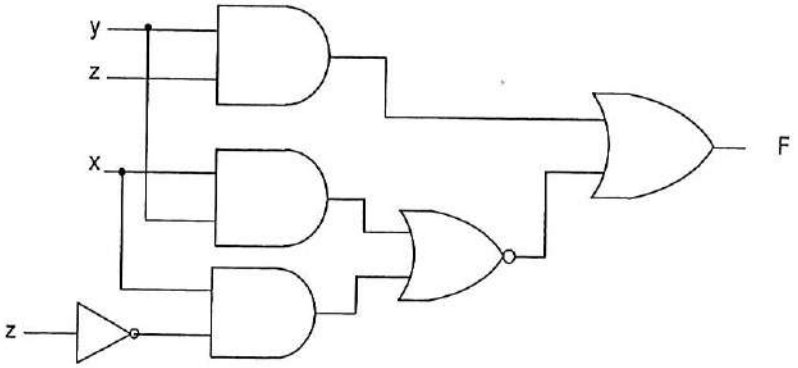


Figure Q2(c) / *Rajah Q2(c)*

i. construct a truth table for function F.
hasilkan jadual kebenaran bagi fungsi F.

ii. What is the minimum number of logic gates required if the circuit is to be converted using NAND gates ONLY?. Show the work clearly.
Apakah bilangan get minimum yang diperlukan jika menukarkan litar tersebut dengan menggunakan get TAK-DAN sahaja?.Tunjukkan jalan kerja dengan jelas.

(7 marks/*markah*)

Q3 (a) Design a logic circuit that has 4 inputs, A (MSB), B, C and D and the output, Y is HIGH as long as input C and D are whether both LOW or both HIGH.

Rekakan litar logik yang mempunyai 4 masukan A (MSB), B, C dan D dan keluaran Y adalah TINGGI selagi masukan C dan D sama ada kedua-duanya adalah TINGGI atau kedua-duanya adalah RENDAH.

(12 marks/*markah*)

(b) Refer Figure Q3(b)(i), draw the output waveforms of 74147 encoder based on input waveform of $\overline{I_3}$,$\overline{I_4}$ and $\overline{I_5}$ in Figure Q3(b)(ii) in attachment sheet. Assumed that other input $\overline{I_1}=\overline{I_2}=\overline{I_6}=\overline{I_7}=\overline{I_8}=\overline{I_9}=1$.

Rujuk Rajah Q3(b)(i), lukiskan gelombang keluaran bagi pengekod 74147 merujuk kepada gelombang masukan bagi $\overline{I_3}$,$\overline{I_4}$ dan $\overline{I_5}$ dalam Rajah Q3(b)(ii) dalam helaian lampiran. Anggap masukan yang lain adalah $\overline{I_1}=\overline{I_2}=\overline{I_6}=\overline{I_7}=\overline{I_8}=\overline{I_9}=1$.

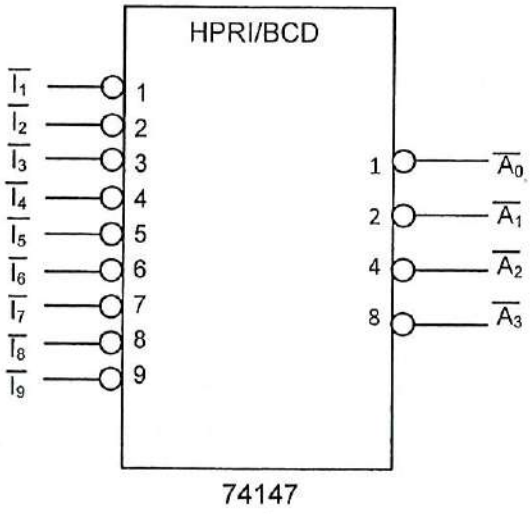


Figure Q3(b)(i) / *Rajah Q3(b)(i)*

(8 marks/*markah*)

Q4 (a) Refer Figure Q4(a), list the appropriate input combination of A, B, C and R for LED always ON.

Rujuk Rajah Q4(a), senaraikan kombinasi masukan yang sesuai bagi A, B, C dan R supaya LED sentiasa HIDUP.

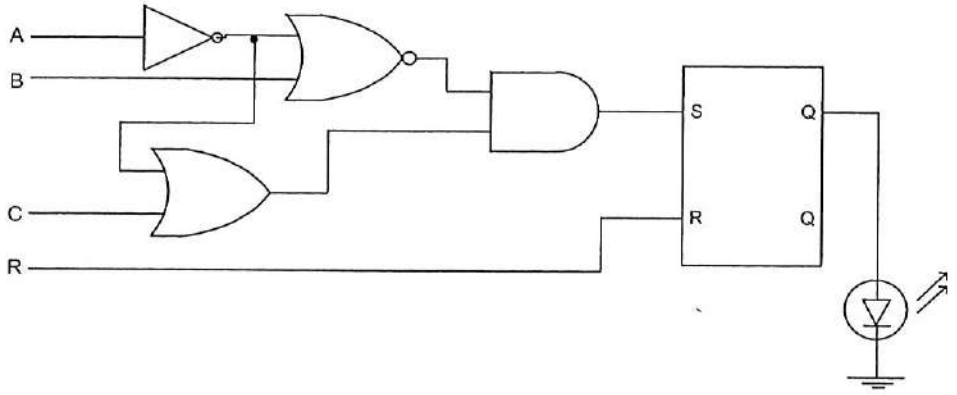


Figure Q4(a) / *Rajah Q4(a)*

(6 marks/*markah*)

(b) With an aid of diagram, give a differences of synchronous and asynchronous counter.

Dengan bantuan gambar rajah, berikan perbezaan di antara pembilang segerak dan pembilang tidak segerak.

(2 marks/*markah*)

(c) Figure Q4(c)(iv) is an IC 74194 bidirectional universal shift register.

Rajah Q4(c)(iv) adalah IC 74194 daftar anjak universal dwihala.

i. Is the CLR input asynchronous or synchronous?

Adakah masukan CLR adalah segerak atau tidak segerak?

ii. What happen to the output if CLK is in LOW condition?

Apakah yang berlaku kepada keluaran jika CLK dalam keadaan RENDAH?

iii. Draw the output waveform in Figure Q4(c)(v) in attachment sheet based on the input given.

Lukiskan gelombang keluaran dalam Rajah Q4(c)(v) dalam helaian lampiran merujuk kepada masukan yang diberikan

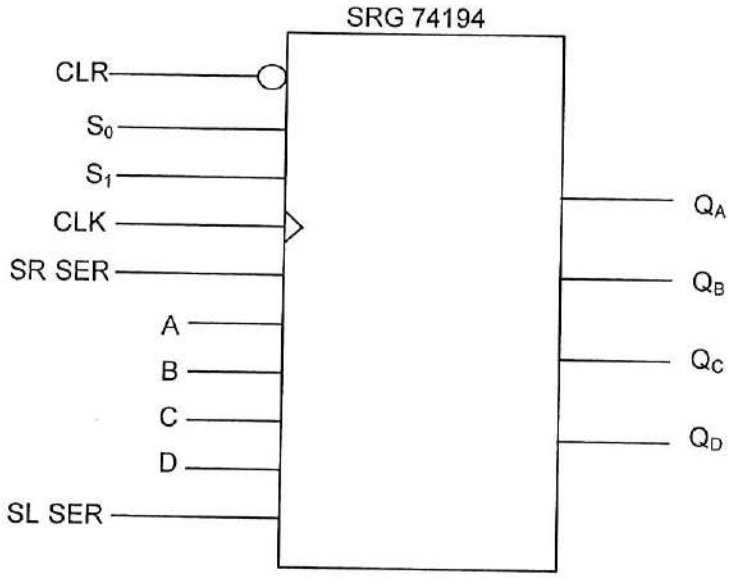


Figure Q4(c)(iv) / *Rajah Q4(c)(iv)*

(12 marks/*markah*)

Q5. (a) What does CMOS and TTL stand for?
Apakah maksud bagi CMOS dan TTL?

(4 marks/*markah)*

(b) A gate produce current of 0.5 mA when the output is HIGH and 15 mA when the output is LOW. Given V_{CC} = +5.5 V and propagation delay of 15 ns, calculate the value of:

i) average current.
ii) power dissipation.
iii) speed-power product

Satu get menghasilkan arus sebanyak 0.5 mA apabila keluaran TINGGI dan 15 mA semasa keluaran RENDAH. Diberi V_{CC} = +5.5 V dan lengahan perambatan, 15 ns, kirakan nilai :

i) arus purata
ii) kuasa lesapan.
iii) hasil darab halaju-kuasa

(6 marks/*markah)*

(c) Determine the values of noise margin (HIGH & LOW) from the logic level shown in Figure Q5(c).

Tentukan nilai bagi jidar hingar (TINGGI & RENDAH) daripada aras logik dalam Rajah Q5(c).

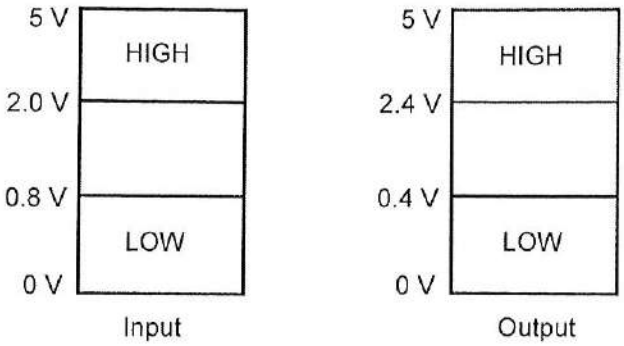


Figure Q5(c) / *Rajah Q5(c)*

(4 marks /*markah*)

(d) State the following terms :-

i. Noise immunity.

ii. Fan-Out.

iii. Propagation delay.

Nyatakan istilah-istilah berikut.

i. Imuniti hingar.

ii. Rebak keluar.

iii. Lengah perambatan.

(6 marks /*markah*)

SN54147, SN54148, SN54LS147, SN54LS148
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS

SDLS053B – OCTOBER 1976 – REVISED MAY 2004

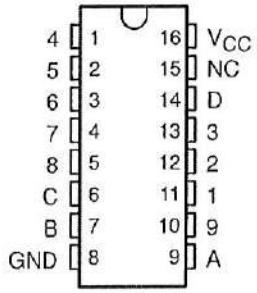
'147, 'LS147

- Encode 10-Line Decimal to 4-Line BCD
- Applications Include:
  - Keyboard Encoding
  - Range Selection

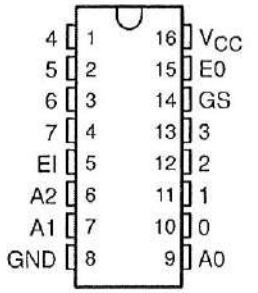
'148, 'LS148

- Encode 8 Data Lines to 3-Line Binary (Octal)
- Applications Include:
  - n-Bit Encoding
  - Code Converters and Generators

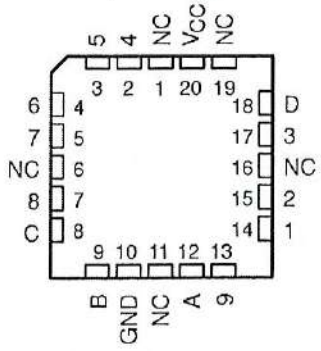
SN54147, SN54LS147 . . . J OR W PACKAGE
SN74147, SN74LS147 . . . D OR N PACKAGE
(TOP VIEW)



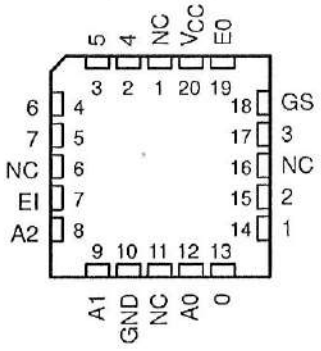
SN54148, SN54LS148 . . . J OR W PACKAGE
SN74148, SN74LS148 . . . D, N, OR NS PACKAGE
(TOP VIEW)



SN54LS147 . . . FK PACKAGE
(TOP VIEW)



SN54LS148 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

TYPE	TYPICAL DATA DELAY	TYPICAL POWER DISSIPATION
'147	10 ns	225 mW
'148	10 ns	190 mW
'LS147	15 ns	60 mW
'LS148	15 ns	60 mW

NOTE: The SN54147, SN54LS147, SN54148, SN74147, SN74LS147, and SN74148 are obsolete and are no longer supplied.

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TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54147, SN54148, SN54LS147, SN54LS148
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS

SDLS053B – OCTOBER 1976 – REVISED MAY 2004

description/ordering information

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The '147 and 'LS147 devices encode nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition, as zero is encoded when all nine data lines are at a high logic level. The '148 and 'LS148 devices encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level. All inputs are buffered to represent one normalized Series 54/74 or 54/74LS load, respectively.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74LS148N	SN74LS148N
	SOIC – D	Tube	SN74LS148D	LS148
		Tape and reel	SN74LS148DR	
	SOP – NS	Tape and reel	SN74LS148NSR	74LS148
–55°C to 125°C	CDIP – J	Tube	SNJ54LS148J	SNJ54LS148J
	CFP – W	Tube	SNJ54LS148W	SNJ54LS148W
	LCCC – FK	Tube	SNJ54LS148FK	SNJ54LS148FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE – '147, 'LS147

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = high logic level, L = low logic level, X = irrelevant

SDLS075

SN54194, SN54LS194A, SN54S194, SN74194, SN74LS194A, SN74S194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

MARCH 1974—REVISED MARCH 1988

- Parallel Inputs and Outputs
- Four Operating Modes:
  - Synchronous Parallel Load
  - Right Shift
  - Left Shift
  - Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overriding Clear

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'194	36 MHz	195 mW
'LS194A	36 MHz	75 mW
'S194	105 MHz	425 mW

description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

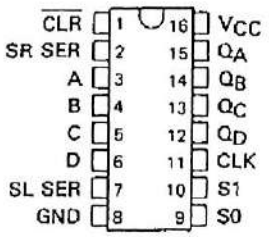
- Inhibit clock (do nothing)
- Shift right (in the direction Q_A toward Q_D)
- Shift left (in the direction Q_D toward Q_A)
- Parallel (broadside) load

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

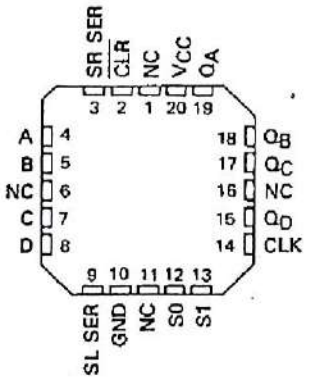
Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the shift register is inhibited when both mode control inputs are low. The mode controls of the SN54194/SN74194 should be changed only while the clock input is high.

SN54194, SN54LS194A, SN54S194 . . . J OR W PACKAGE
SN74194 . . . N PACKAGE
SN74LS194A, SN74S194 . . . D OR N PACKAGE
(TOP VIEW)

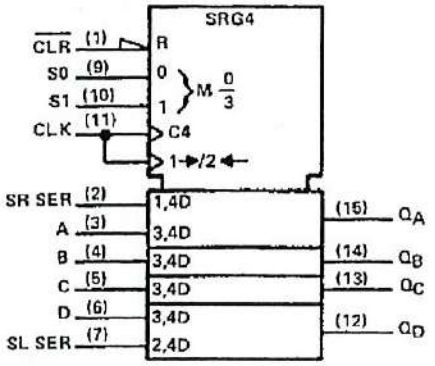


SN54LS194A, SN54S194 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

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SN54194, SN54LS194A, SN54S194
SN74194, SN74LS194A, SN74S194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

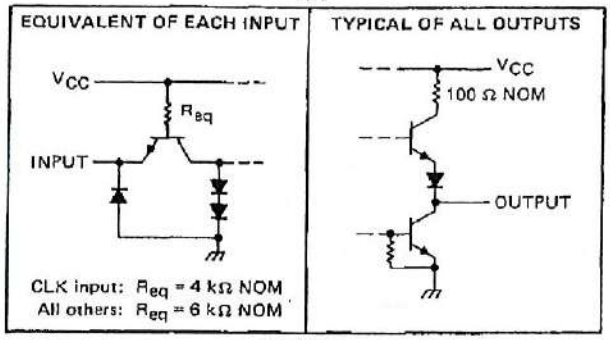
FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

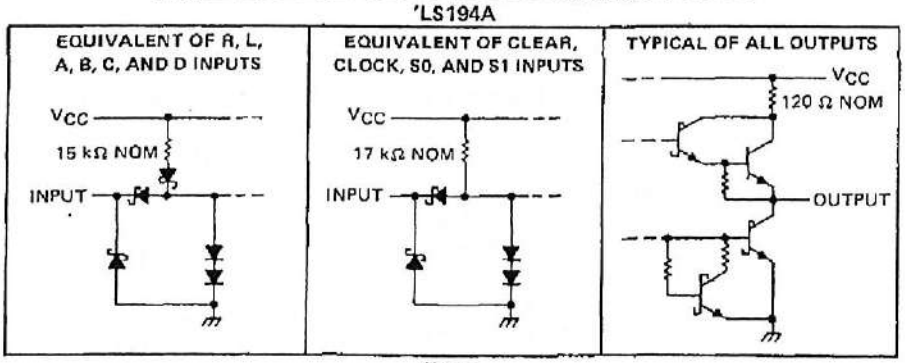
H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

schematics of inputs and outputs

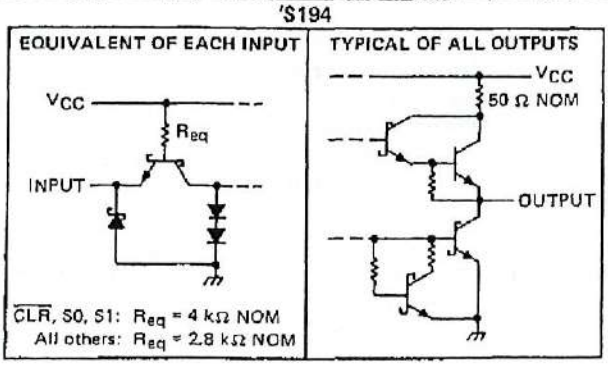
'194



'LS194A



'S194



Attachment / *Lampiran*

Name:_____

ID Number:_____

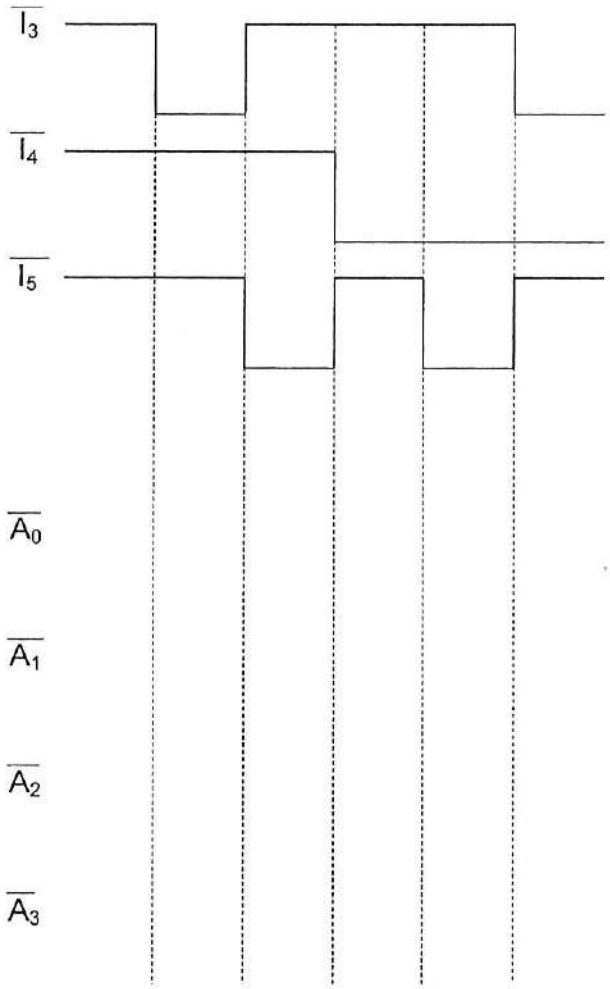


Figure Q3(b)ii / *Rajah Q3(b)ii*

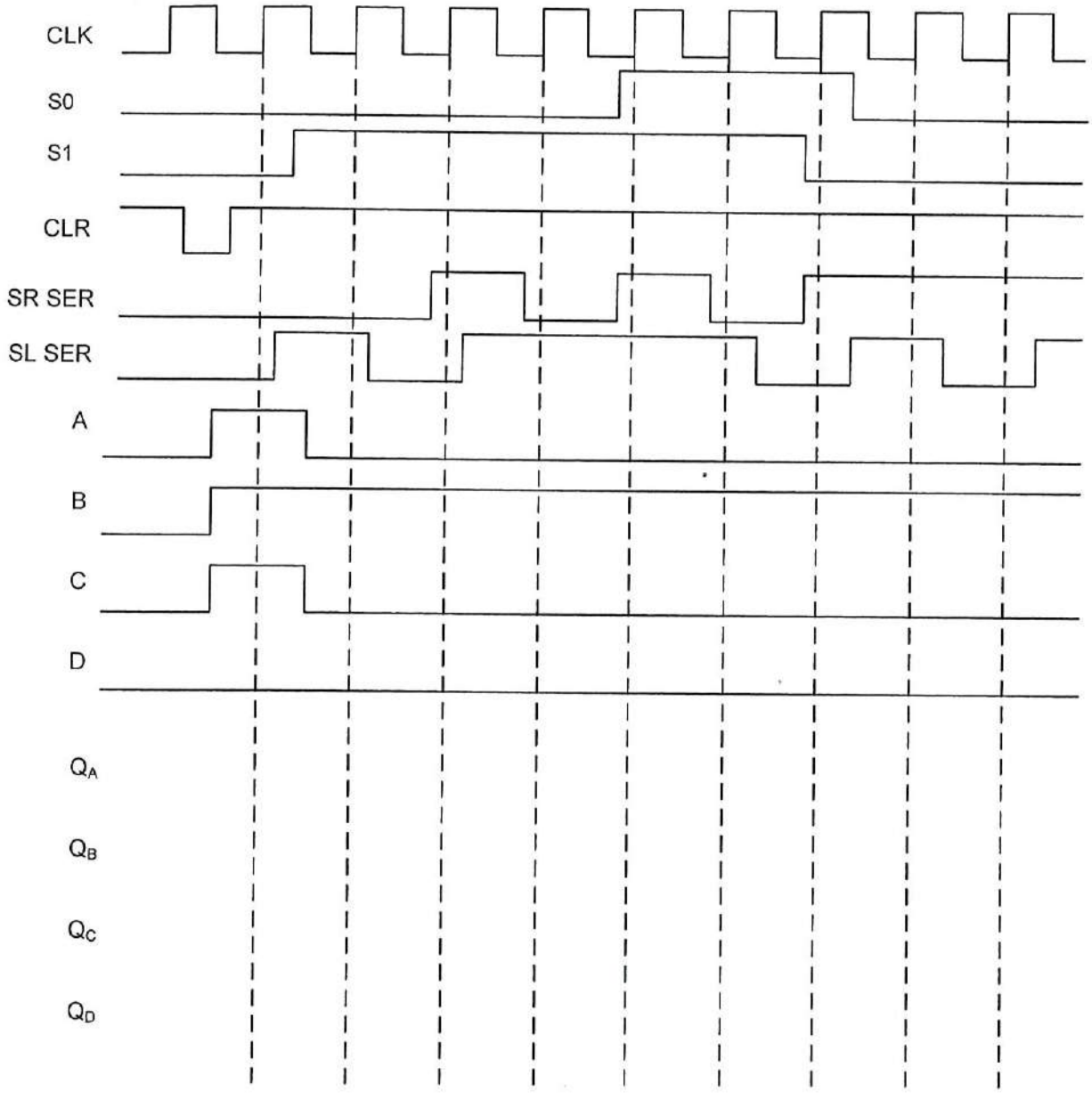


Figure Q4(c)(v) / *Rajah Q4(c(v)*

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