KOLEJ YAYASAN PELAJARAN JOHOR

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FINAL EXAMINATION

COURSE NAME	:	**ADVANCE DIGITAL**
COURSE CODE	:	**DEE 2013**
EXAMINATION	:	**APRIL 2018**
DURATION	:	**2 HOURS 30 MINUTES**

INSTRUCTION TO CANDIDATES

1. This examintaion paper consists **FIVE (5)** questions. Answer **ALL** questions in the answer booklet provided.

2. Candidates are not allowed to bring any material to examination room except with the permission from the invigilator.

3. Please check to make sure that this examination pack consist of:
   i. Question Paper
   ii. Answer Booklet

DO NOT TURN THIS PAGE UNTIL YOU ARE TOLD TO DO SO

This examination paper consists of 14 printed pages including front page

This part contains of **FIVE(5)** questions. Answer **ALL** questions in the answer booklet provided.

*Bahagian ini mengandungi **LIMA (5)** soalan. Jawab **SEMUA** soalan di dalam buku jawapan yang disediakan.*

QUESTION 1/SOALAN 1

a) State **one (1)** difference between a bistable multivibrator and an astable multivibrator.

*Nyatakan **satu (1)** perbezaan antara pemberbilang getar dwistabil dengan pemberbilang getar tak stabil.*

(2 marks/*markah*)

b) Given the output frequency of an oscillator using a 555 timer IC is 2.2 kHz. Calculate the output duty cycle if t_L is 0.2ms.

Diberi frekuensi keluaran bagi sebuah pengayun menggunakan serpih pemasa 555 adalah 2.2 kHz. Kirakan kitar tugas bagi keluaran jika t_L adalah 0.2ms.

(3 marks/*markah*)

c) Figure Q1(c)(i) in attachment shows a basic digital circuit comprising of edge-triggered J-K flip-flops with the PRESET and CLEAR inputs. Draw the output waveforms for Q_1 and Q_2 in Figure Q1(c)(ii) in the attachment. Assume all flip-flop outputs are initially LOW.

Rajah Q1(c)(i) dalam lampiran menunjukkan satu litar digital yang mengandungi flip-flop J-K terpicu pinggir dengan masukan PRESET dan CLEAR. Lukiskan gelombang keluaran untuk Q_1 dan Q_2 dalam Rajah Q1(c)(ii) dalam lampiran . Anggapkan kesemua keluaran flip-flop pada awalnya adalah RENDAH.

(8 marks/*markah*)

d) Referring to the Figure Q1(d)(i), draw the output Q_A and Q_B in Figure Q1(d)(ii). Assume all flip flop outputs are initially LOW.

Merujuk kepada Rajah Q1(d)(i), lukiskan keluaran Q_A dan Q_B dalam Rajah Q1(d)(ii).Anggapkan kesemua keluaran flip flop adalah RENDAH pada awalnya.

(7 marks/*markah*)

QUESTION 2/SOALAN 2

a) State **two (2)** differences between synchronous and asynchronous counters.

*Berikan **dua (2)** perbezaan diantara pembilang segerak dan pembilang tak segerak.*

(4 marks/*markah*)

b) Figure Q2(b)(i) in attachment shows an IC 74LS93 used for asynchronous counter design. Draw the connection for MOD 14 counter.

Rajah Q2(b)(i) dalam lampiran ialah satu IC 74LS93 yang digunakan untuk rekabentuk pembilang tak segerak. Lukiskan sambungan untuk pembilang MOD14.

(6 marks/*markah*)

c) Refer Figure Q2(c) in attachment, draw the output waveform for Q_0, Q_1, Q_2 and Q_3 and state the sequence for the 4 bits $UP / \overline{DOWN}$ counter referring the given input. The starting state for the counter is '0' with positive edge triggered.

Rujuk Rajah Q2(c) di dalam lampiran, lukiskankan gelombang keluaran bagi Q_0, Q_1, Q_2 and Q_3 dan tentukan turutan bagi pembilang segerak binary $NAIK / \overline{TURUN}$ 4-Bit merujuk kepada masukan yang diberikan. Pembilang bermula dengan keadaan '0' dengan picuan tepi positif.

(10 marks/*markah*)

QUESTION 3 /SOALAN 3

a) How many flip flops are needed to design the following counters.
Berapa banyakkah bilangan flip flop diperlukan untuk mereka pembilang ini.

i) MOD 128 Binary counter.
Pembilang Binari MOD 128. (2 marks/*markah*)

ii) MOD 128 Johnson counter.
Pembilang Johnson MOD 128. (2 marks/*markah*)

iii) MOD 128 Ring counter.
Pembilang Gelang MOD 128. (2 marks/*markah*)

b) Figure Q3(b)(i) shows a 3 bits ring counter circuit. If the initial state is 101, draw the output waveforms in Figure Q3(b)(ii) for each of the flip flop output for 7 clock pulse.

Rajah Q3(b)(i)menunjukkan satu pembilang gelang 3 bit. Jika keadaan awal adalah 101, lukis gelombang keluaran dalam Rajah Q3(b)(ii) untuk setiap keluaran flip flop bagi 7 denyut jam.

(6 marks/*markah*)

c) For the 10-bits serial-in/serial-out shift (SISO) register shown in Figure Q3(c)(i), sketch the data output waveform Q_{10}, for the data input and clock pulse in Figure Q3(c)(ii).Assume that the register is inially LOW.

Bagi daftar anjak 10-bit masuk siri/keluar siri (SISO) yang ditunjukkan dalam Rajah Q3(c)(i), lakarkan gelombang keluaran Q_{10},berdasarkan data masukan dan denyut jam pada Rajah Q3(c)(ii). Anggap keadaan awal daftar adalah RENDAH.

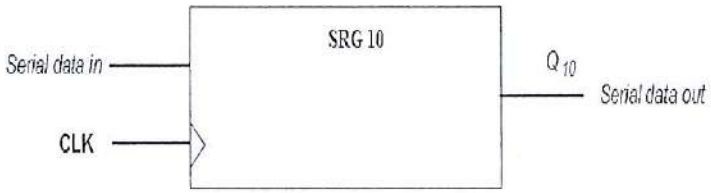


Figure Q3(c)(i)/ *Rajah Q3(c)(i)*

(8 marks/*markah*)

QUESTION 4/SOALAN 4

a) Name the DAC circuit given in Figure Q4(a)(i) and Q4(a)(ii).
Namakan litar DAC yang diberikan pada Rajah Q4(a)(i) dan Q4(a)(ii).

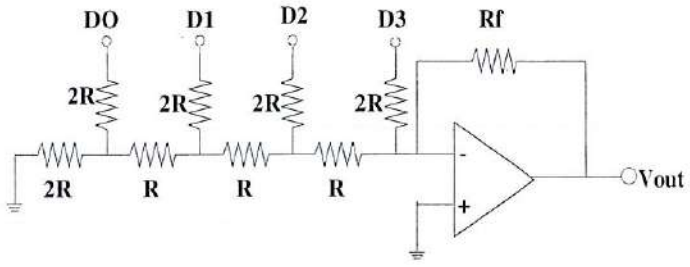


Figure Q4(a)(i)/ Rajah Q4(a)(i)

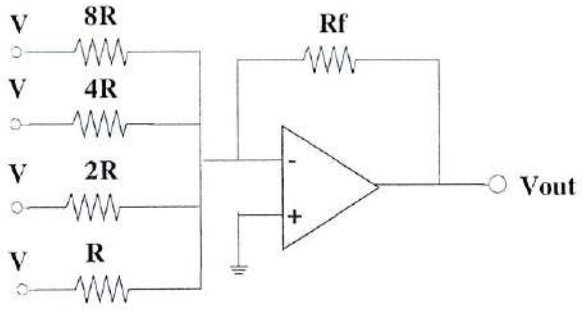


Figure Q4(a)(ii)/ Rajah Q4(a)(ii)

(4 marks/markah)

b) Calculate the percentage resolution for 8-bit Digital to Analog Converter (DAC).
Kirakan peratus resolusi bagi sebuah penukar Digital to Analog (DAC) 8-bit.

(2 marks/markah)

c) A certain DAC will produce 5.0 V if a digital input is 01000010_2. Determine
Sebuah DAC akan menghasilkan keluaran 5.0 V jika masukan digital ialah 01000010_2. Tentukan

i- resolution of the DAC.
resolusi DAC tersebut. (2 marks/markah)

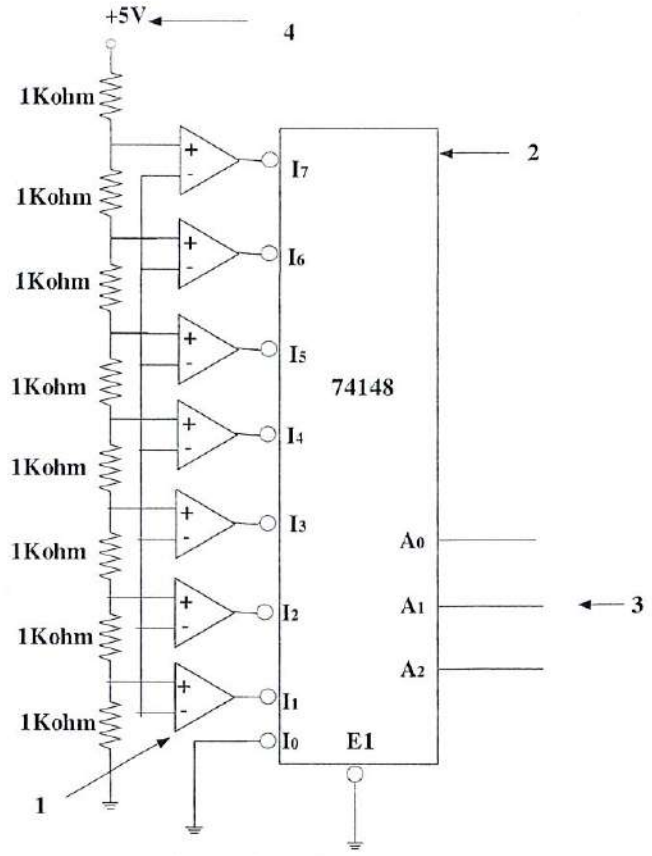
ii- the largest value of output voltage (Vout) from an eight bit DAC .
nilai terbesar bagi voltan keluaran (Vout) daripada penukar DAC 8 bit.
(2 marks/markah)

iii- percentage of resolution.
peratus resolusi.
(2 marks/markah)

d)

i- Name the converter circuit as shown in Figure Q4(d).
Namakan litar penukar yang ditunjukkan dalam Rajah Q4(d).
(2 marks/markah)

ii- State the name of elements labeled in the circuit
Nyatakan nama elemen-elemen yang dilabelkan dalam litar tersebut.
(2 marks/markah)



e)

Figure Q4(d)/ *Rajah Q4(d)*

iii- State how many comparators would a 12 bits converter in Q4(d)(i) required? How many resistors needed?

Nyatakan berapa banyakkah pembanding diperlukan untuk penukar dalam Q4(d)(i) 12 bit. Berapa banyak perintang diperlukan?

(4 marks/markah)

QUESTION 5/SOALAN 5

a) Define each following term in memory terminology below:
Takrifkan istilah didalam terminologi ingatan di bawah :

i) byte.
bait.

ii) capacity,
kapasiti.

(2 marks/*markah)*

b) A certain memory has a capacity 32K x 8.
Suatu ingatan mempunyai kapasiti 32 K x 8.

i) Find how many data input and data output lines does it have.
Dapatkan bilangan masukan data dan keluaran data yang diperlukan untuk ingatan itu.
(2 marks/markah)

ii) Calculate how many address input does it have.
Kirakan bilangan masukan alamat yang diperlukan untuk ingatan itu.
(2 marks/markah)

iii) Find the capacity in bytes?
Dapatkan kapasiti ingatan didalam bait?
(2 marks/markah)

c) A memory system is implemented as shown in Figure Q5(c).
Sebuah sistem ingatan dilaksanakan seperti dalam Rajah Q5(c).

i) Determine the lowest and the highest address of each RAM module in hexadecimal. Produce the address table.
Tentukan alamat terendah dan alamat tertinggi bagi setiap modul RAM dalam hexadecimal. Hasilkan jadual alamat.
(10 marks/markah)

ii) Determine the capacity of the memory system.
Tentukan kapasiti sistem ingatan berkenaan.
(2 marks/markah)

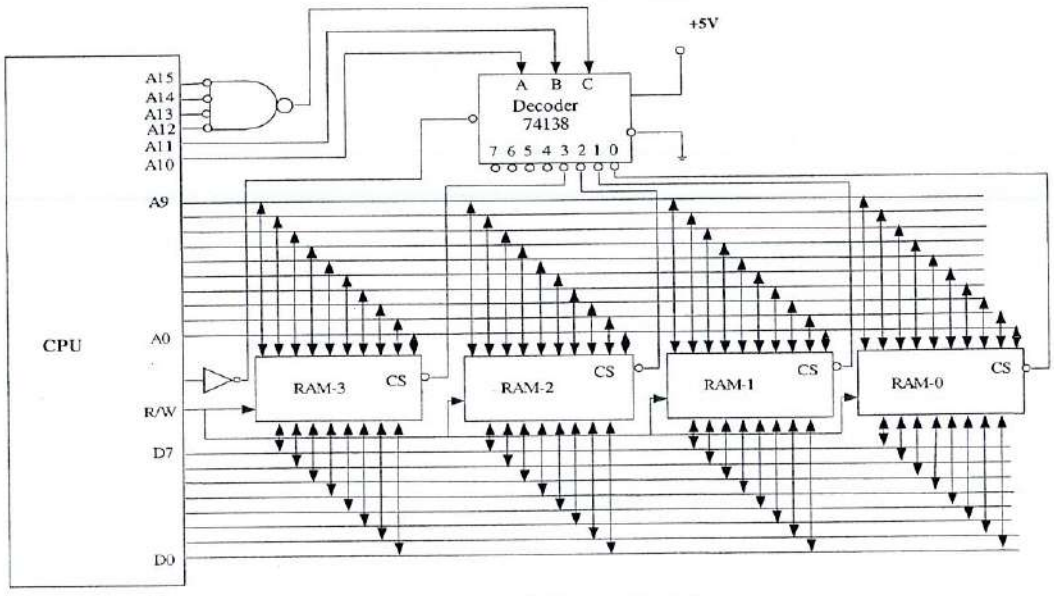


Figure Q5(c)/ *Rajah Q5(c).*

(100 MARK/MARKAH)

ATTACHMENT/LAMPIRAN

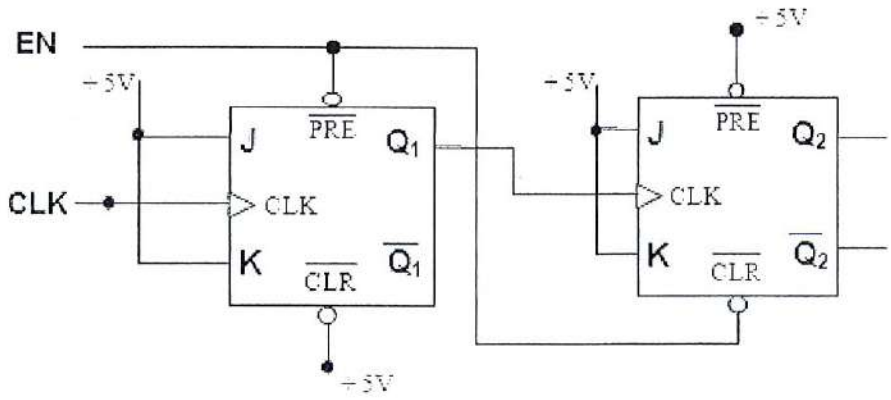


Figure Q1(c)(i) / *Rajah Q1(c)(i)*

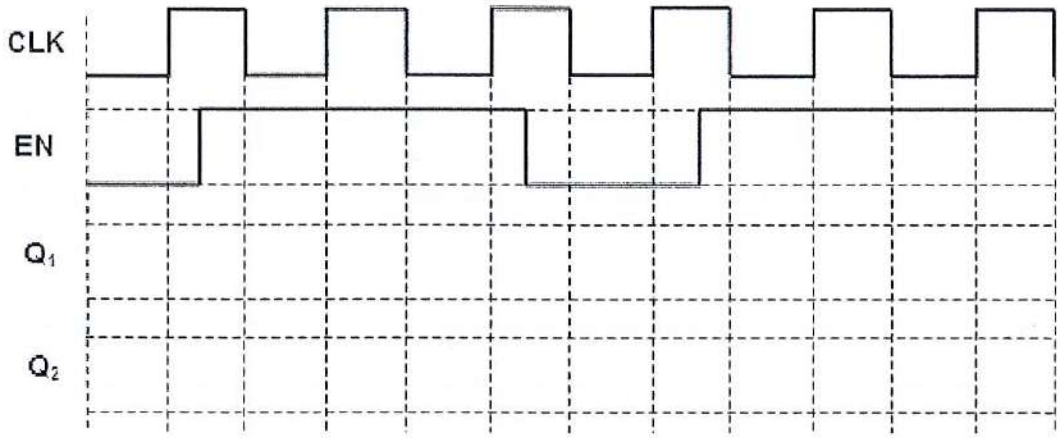


Figure Q1(c)(ii) / *Rajah Q1(c)(ii)*

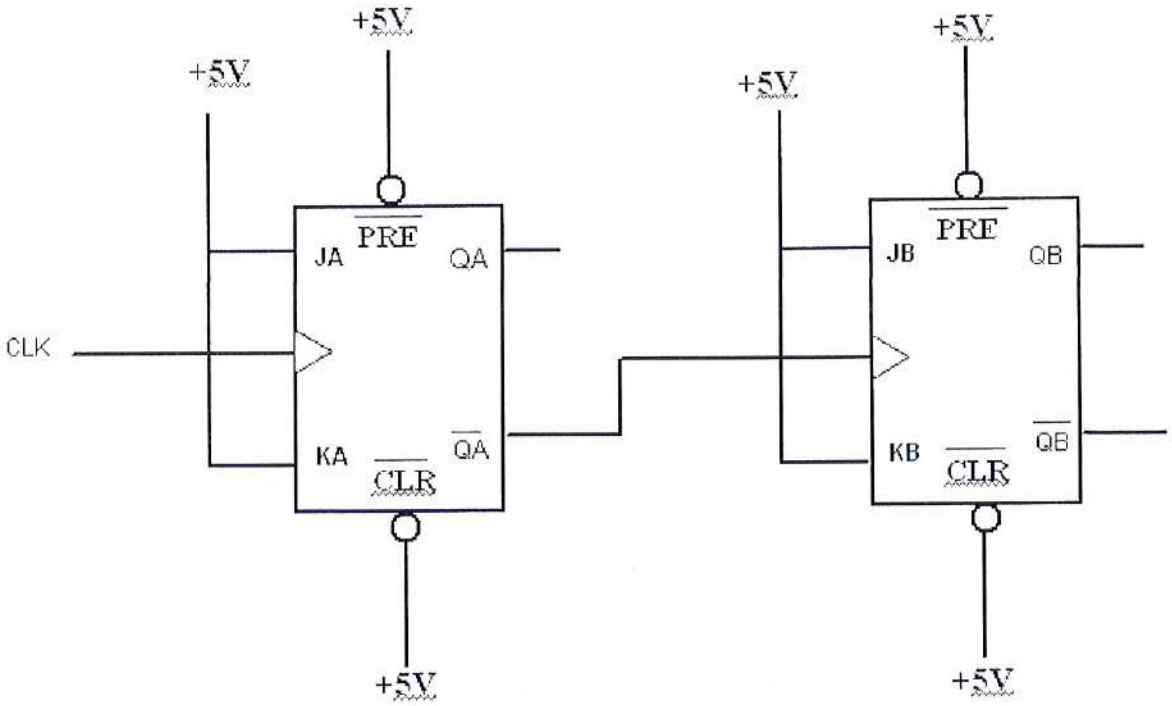


Figure Q1(d)(i)/ *Rajah Q1(d)(i)*

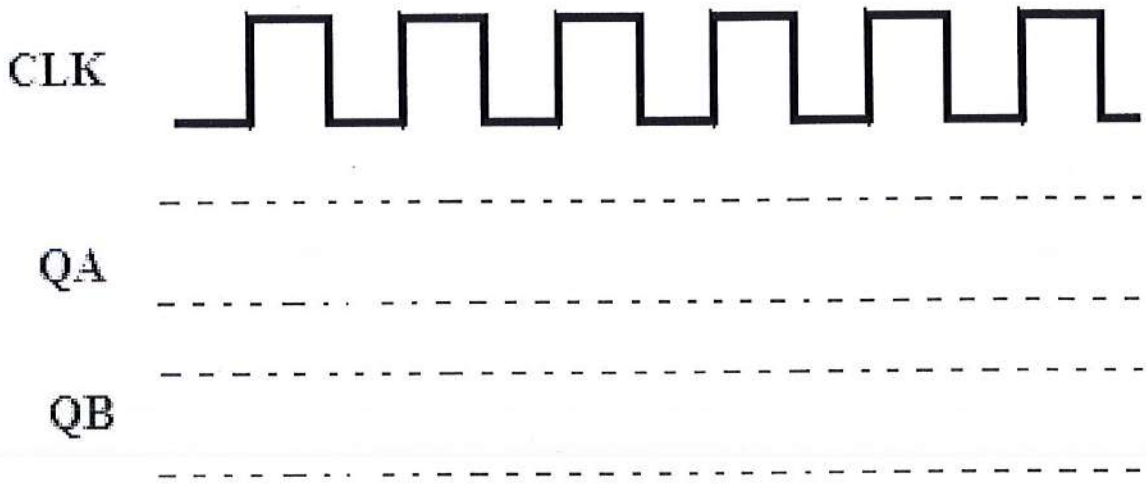


Figure Q1(d)(ii)/ *Rajah Q1(d)(ii)*

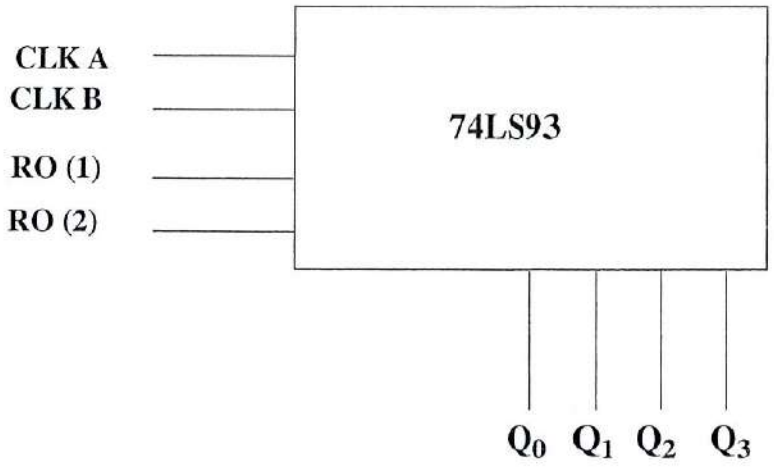


Figure Q2(b)(i)/ *Rajah Q2(b)(i)*

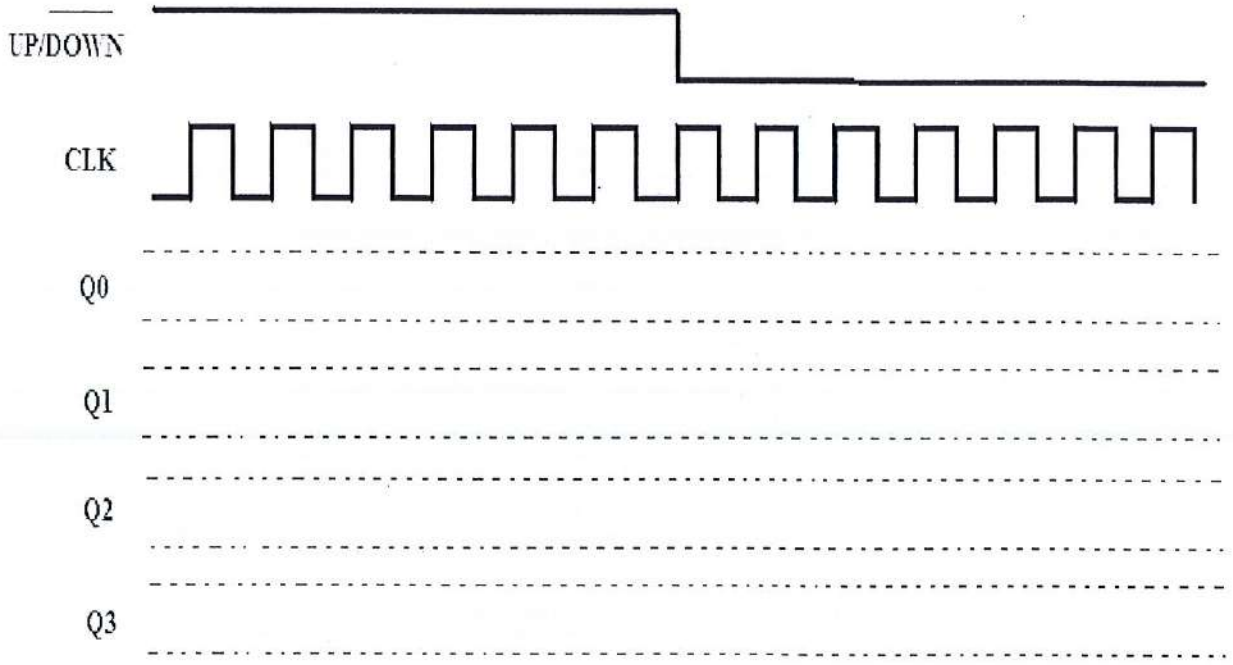


Figure Q2(c)/ *Rajah Q2(c)*

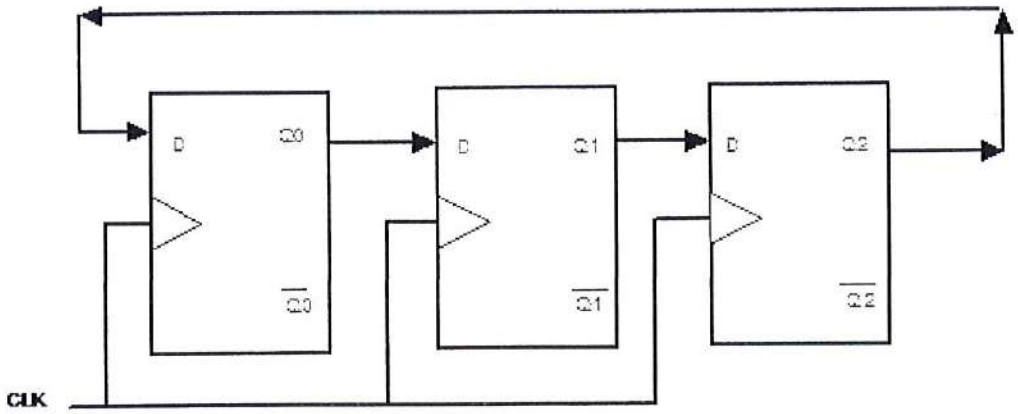


Figure Q3(b)(i)/ *Rajah Q3(b)(i)*

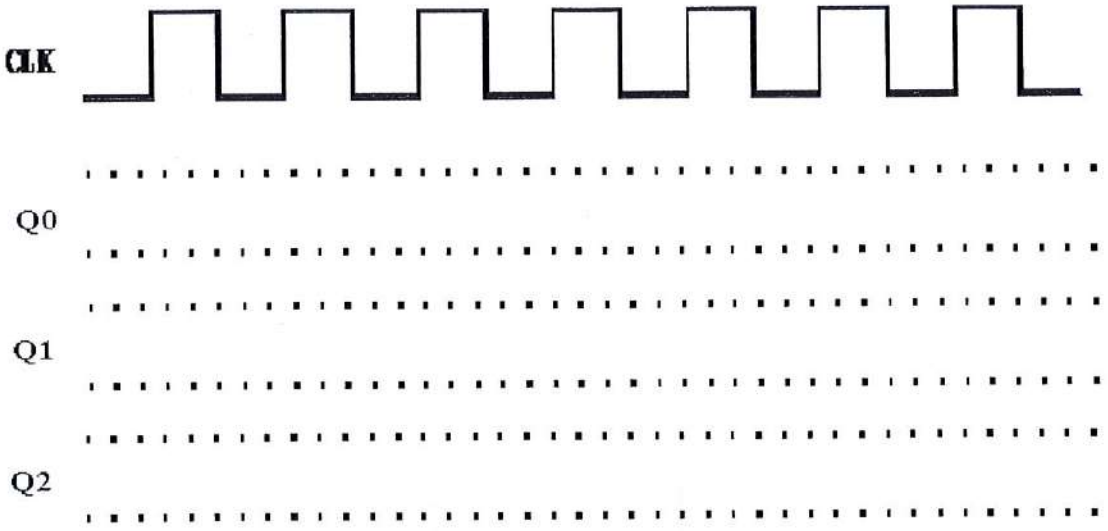


Figure Q3(b)(ii)/ *Rajah Q3(b)(ii)*

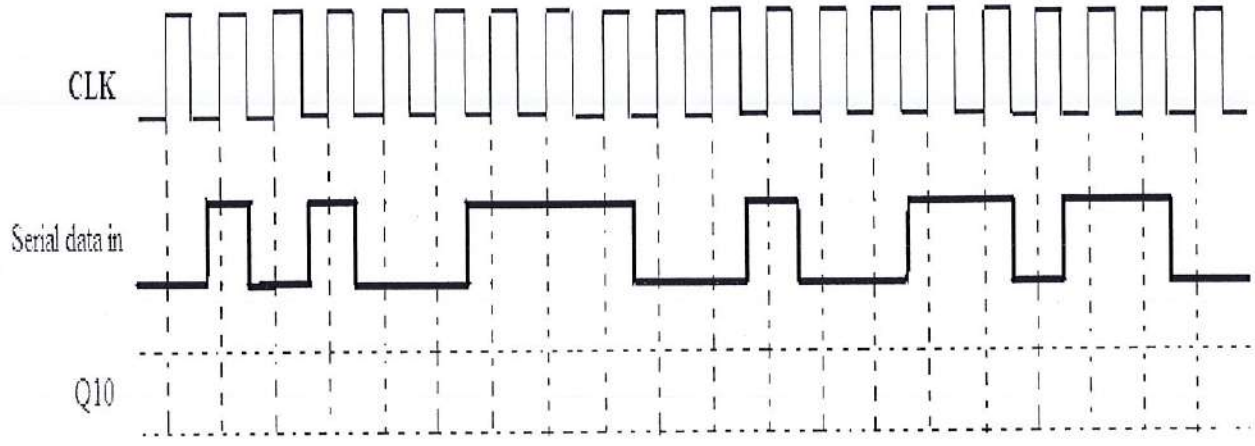


Figure Q3(c)(ii)/ *Rajah Q3(c)(ii)*

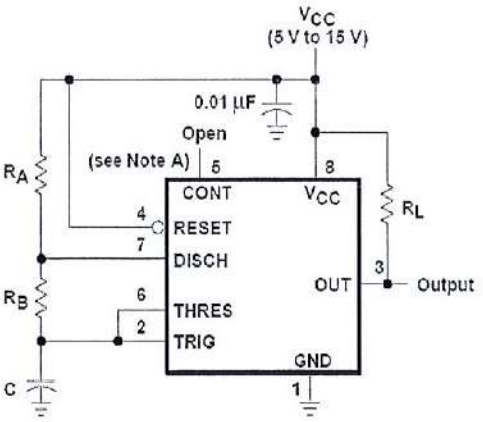
END OF QUESTION PAPER/KERTAS SOALAN TAMAT

APPLICATION INFORMATION

astable operation

As shown in Figure 12, adding a second resistor, R_B, to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \times V_{CC}$) and the trigger-voltage level ($\approx 0.33 \times V_{CC}$). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 12. Circuit for Astable Operation

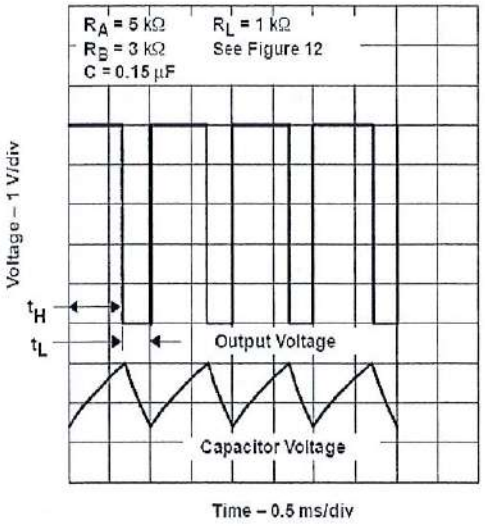


Figure 13. Typical Astable Waveforms

Figure 13 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L can be calculated as follows:

$$t_H = 0.693\ (R_A + R_B)\ C$$

$$t_L = 0.693\ (R_B)\ C$$

Other useful relationships are shown below.

$$\text{period} = t_H + t_L = 0.693\ (R_A + 2R_B)\ C$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)\ C}$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B}$$

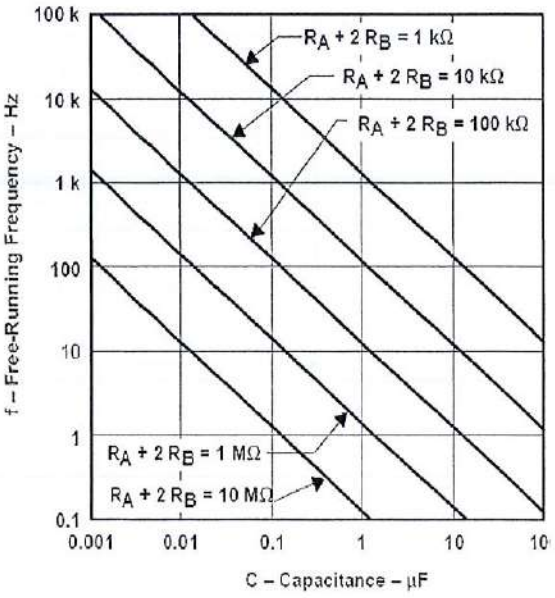
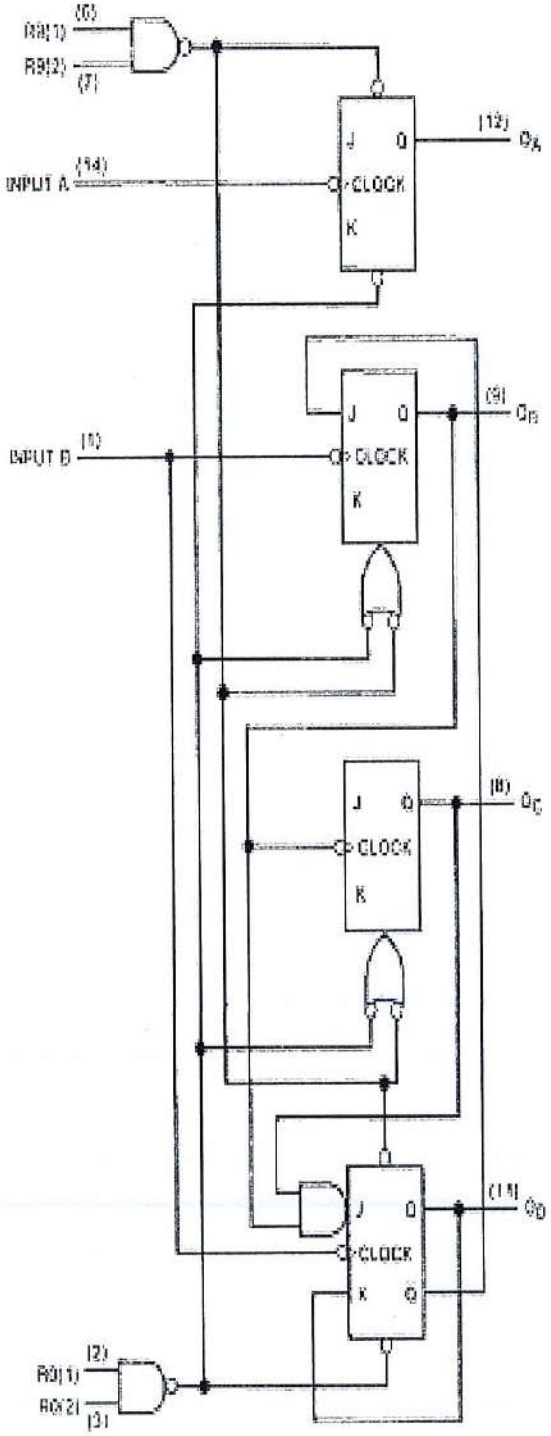


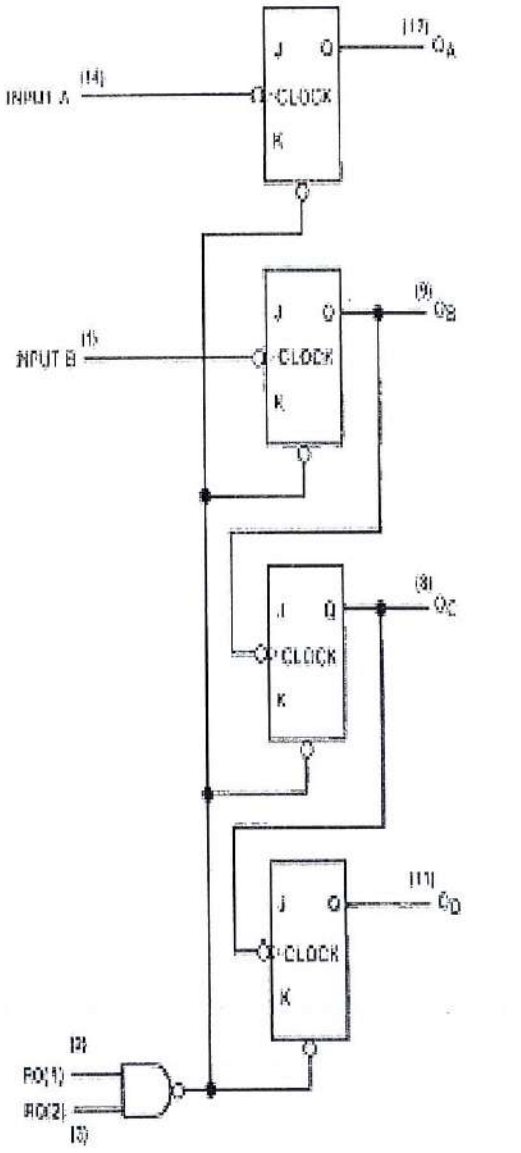
Figure 14. Free-Running Frequency

Logic Diagrams

LS90



LS93



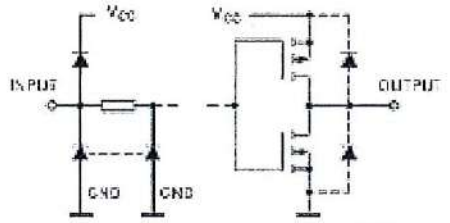
TL/F/6381-4

TL/F/6381-3

The J and K inputs shown without connection are for reference only and are functionally at a high level.

M54/M74HC164

INPUT AND OUTPUT EQUIVALENT CIRCUIT



TRUTH TABLE

INPUTS				OUTPUTS			
CLEAR	CLOCK	SERIAL IN		QA	QB	.....	QH
		A	B				
L	X	X	X	L	L	.....	L
H	⊓	X	X	NO CHANGE			
H	⊔	H	X	H	QAn	.....	QGn
H	⊔	X	L	L	QAn	.....	QGn
H	⊔	H	H	H	QAn	.....	QGn

X: Don't Care
QAn - QGn : The level of QA-QG respectively before the most recent transition of the clock.

LOGIC DIAGRAM