KOLEJ YAYASAN PELAJARAN JOHOR

**KOLEJ YAYASAN PELAJARAN JOHOR**
**FINAL EXAMINATION**

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|---|---|---|
| **COURSE NAME** | : | **ELECTRONIC CIRCUIT** |
| **COURSE CODE** | : | **DEE 1073** |
| **EXAMINATION** | : | **JUNE 2024** |
| **DURATION** | : | **2 HOURS AND 30 MINUTES** |

**INSTRUCTION TO CANDIDATES /**
***ARAHAN KEPADA CALON***

1. This examination paper consists of **ONE (1)** part : / PART A (100 Marks) /
   *Kertas soalan ini mengandungi **SATU (1)** bahagian:* *BAHAGIAN A (100 Markah)*

2. Candidates are not allowed to bring any material to examination room except with the permission from the invigilator. The formula was attached at the back question paper. /
   *Calon tidak dibenarkan untuk membawa sebarang bahan/nota ke bilik peperiksaan tanpa arahan/kebenaran daripada pengawas. Rumus dilampirkan di belakang kertas soalan peperiksaan.*

3. Please check to make sure that this examination pack consists of: /
   *Pastikan kertas soalan peperiksaan ini mengandungi:*
   i. Question Paper /
      *Kertas Soalan*
   ii. Answering Booklet /
      *Buku Jawapan*
   iii. Graph Paper/
      *Kertas Graf*

**DO NOT TURN THIS PAGE UNTIL YOU ARE TOLD TO DO SO /**
***JANGAN BUKA KERTAS SOALAN INI SEHINGGA DIBERITAHU***

This examination paper consists of **10** printed pages including front page
*Kertas soalan ini mengandungi **10** muka surat termasuk kulit hadapan*

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This part contains of **FOUR(4)** questions. Answer **ALL** questions in the Answering Booklet.

*Bahagian ini mempunyai **EMPAT(4)** soalan. Jawab **SEMUA** soalan di dalam Buku Jawapan.*

**QUESTION 1 / *SOALAN 1***

Given $V_{DD}$ = 18V, $R_D$ = 2kΩ, $R_G$ = 1MΩ with $V_{GG}$ = -2V, $I_{DSS}$ = 10 mA and $V_P$ = - 8V for the JFET fixed bias circuit.

a) Draw the complete schematic symbol with fixed bias circuit for N channel JFET.

**(6 marks / *markah*)**

b) From **answer at a)**, sketch the transfer curve for the device. (answer in graph paper)

**(8 marks / *markah*)**

c) Form the graph find,

i) Q-Operating point $I_{DQ}$ and $V_{GSQ}$.

**(5 marks / *markah*)**

ii) Drain voltage, $V_D$.

**(2 marks / *markah*)**

iii) Gate voltage, $V_G$.

**(2 marks / *markah*)**

iv) Drain-to-source voltage, $V_{DSQ}$.

**(2 marks / *markah*)**

*Diberi $V_{DD}$ = 18V, $R_D$ = 2kΩ, $R_G$ = 1MΩ bersama $V_{GG}$ = -2V, $I_{DSS}$ = 10 mA dan $V_P$ = - 8V bagi litar JFET pincang tetap.*

*a) Lukiskan simbol skematik yang lengkap dengan litar pincang tetap bagi JFET saluran N.*

*b) Dari **rajah soalan a)**, lakarkan lengkung pindah bagi peranti (jawab dalam kertas graf)*

*c) Dari graf dapatkan,*

*i) Titik kendalian-Q $I_{DQ}$ dan $V_{GSQ}$.*

*ii) Voltan salir, $V_D$.*

*iii) Voltan get, $V_G$.*

*iv) Voltan salir-sumber, $V_{DSQ}$.*

**QUESTION 2 / *SOALAN 2***

a) Refer to **Figure 2a**,

i) Determine the total voltage gain, $A_{VT}$.

**(3 marks / *markah*)**

ii) Sketch and label $V_{in}$, $V_{o2}$ and $V_o$.

**(3 marks / *markah*)**

b) Refer to **Figure 2b**,

i) Draw and label the ac equivalent circuit.

**(2 marks / *markah*)**

ii) Calculate Zi, Zo, $A_{V1}$, $A_{V2}$ and $A_{VT}$.

**(14 marks / *markah*)**

iii) Sketch and label the output voltage, Vo with reference to the input voltage, Vi.

**(3 marks / *markah*)**

*a) Rujuk pada **Rajah 2a**,*

*i) Tentukan jumlah gandaan voltan , $A_{VT}$.*

*ii) Lakar dan labelkan $V_{in}$, $V_{o2}$ and $V_o$.*

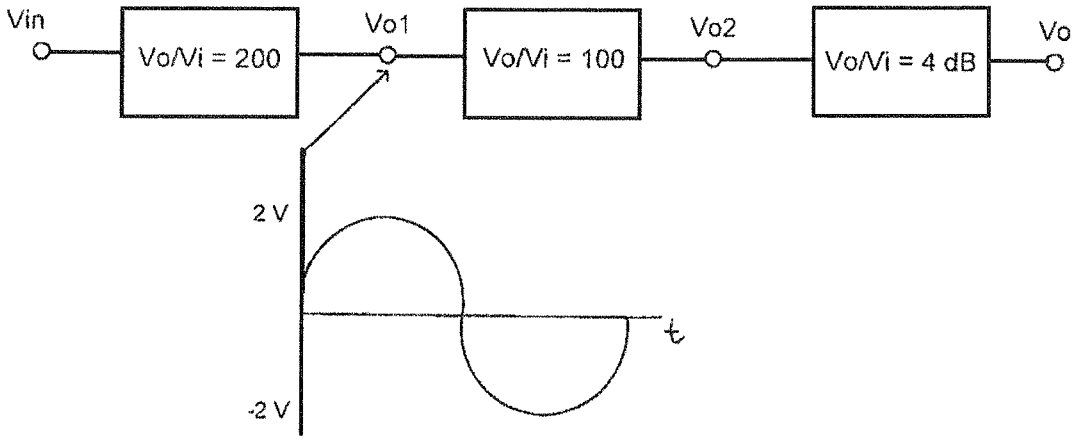


**Figure 2a/ *Rajah 2a***

b) *Rujuk pada **Rajah 2b**,*

*i) Lukis dan labelkan litar setara au.*

*ii) Kirakan Zi, Zo, $A_{V1}$, $A_{V2}$ dan $A_{VT}$.*

*iii) Lakar dan labelkan voltan keluaran, Vo dengan merujuk kepada voltan masukan, Vi.*

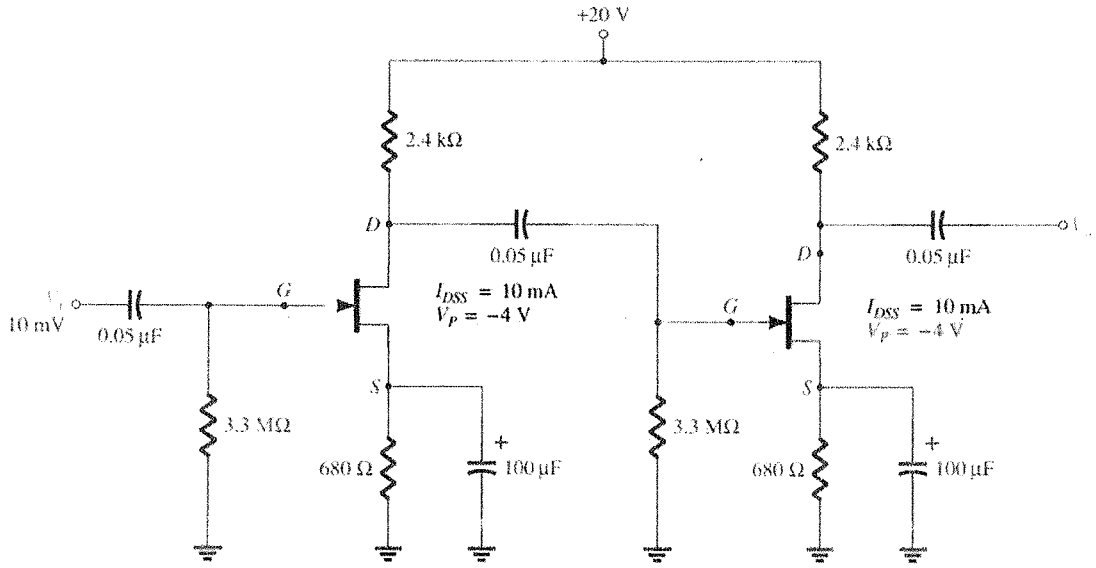


**Figure 2b/ *Rajah 2b***

## QUESTION 3 / *SOALAN 3*

a) Referring to the operational amplifier (Op-Amp) circuit in **Figure 3a**,

i) Named each of amplifier used in this multistage Op-Amp.

**(3 marks / *markah*)**

ii) Determine the output voltage $V_{O1}$, $V_{O2}$ and $V_O$.

**(17 marks / *markah*)**

b) Op-Amp can be used to build active filter. There are few types of filters that are popularly used in many applications.

i) Named three (3) type of active filter.

**(3 marks / *markah*)**

ii) For the filter circuit in **Figure 3b**, sketch the practical frequency response of the filter.

**(2 marks / *markah*)**

*a) Merujuk litar penguat kendalian (Op-Amp) dalam **Rajah 3a**,*

*i) Namakan setiap penguat dalam Op-Amp berbilang tahap.*

*ii) Tentukan voltan keluaran $V_{O1}$, $V_{O2}$ dan $V_O$.*

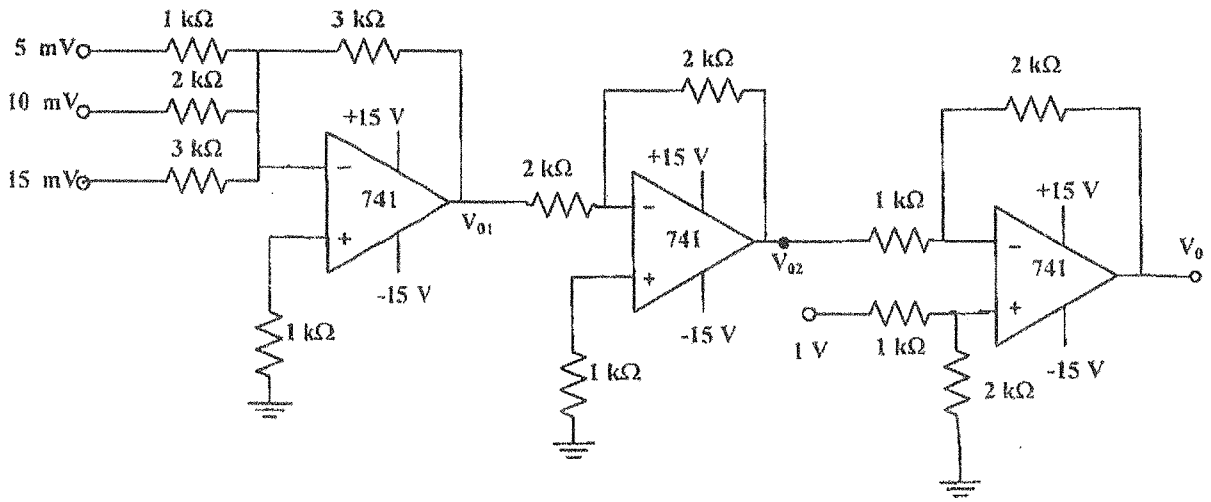


**Figure 3a/ *Rajah 3a***

b) *Op-Amp boleh digunakan untuk membina penapis aktif. Terdapat beberapa jenis penapis yang sangat popular digunakan dalam beberapa aplikasi.*

*i) Namakan tiga (3) jenis penapis aktif.*

*ii) Bagi litar dalam **Rajah 3b**, lakarkan sambutan frekuensi praktikal bagi penapis ini.*

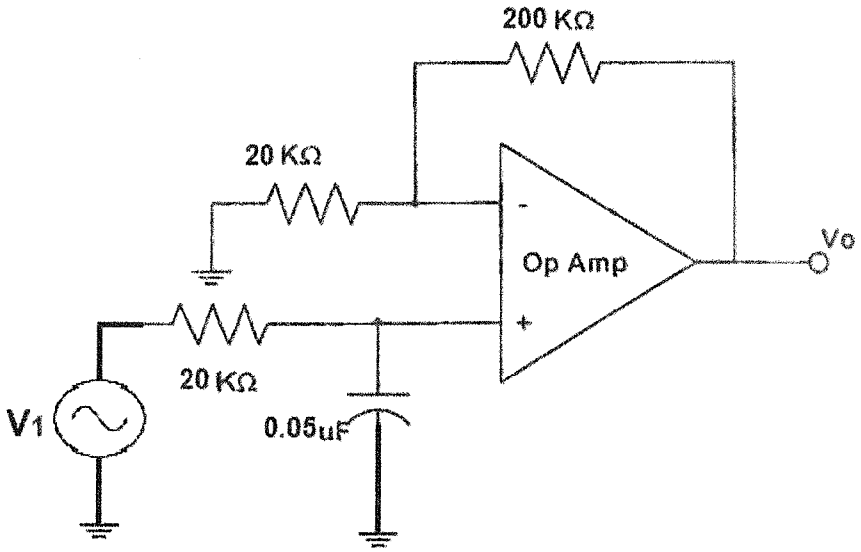


**Figure 3b/ *Rajah 3b***

**QUESTION 4 / *SOALAN 4***

a) List **two (2)** characteristics for each of the following classes of amplifiers.

i) Class A

**(2 marks / *markah*)**

ii) Class B

**(2 marks / *markah*)**

iii) Class AB

**(2 marks / *markah*)**

b) For the circuit of **Figure 4b**, calculate:

i) The input power, $P_{i(dc)}$.

**(5 marks / *markah*)**

ii) Output power, $P_{o(ac)}$.

**(4 marks / *markah*)**

iii) Power handled by each output transistor.

**(2 marks / *markah*)**

iv) The circuit efficiency, % $\eta$.

**(2 marks / *markah*)**

v) Maximum input power, $P_{i(dc)}$.

**(2 marks / *markah*)**

vi) Maximum input power, $P_{o(ac)}$.

**(2 marks / *markah*)**

vii) Maximum efficiency, % $\eta$.

**(2 marks / *markah*)**

*a) Senaraikan dua (2) ciri bagi setiap kelas penguat berikut.*

*i) Kelas A*

*ii) Kelas B*

*iii) Kelas AB*

*b) Bagi litar pada **Rajah 4b**, kirakan:*

*i) Kuasa masukan, $P_{i(dc)}$.*

*ii) Kuasa keluaran, $P_{o(ac)}$.*

*iii) Kuasa kendalian untuk setiap transistor.*

*iv) Kecekapan litar, % $\eta$.*

*v) Kuasa masukan maksimum, $P_{i(dc)}$.*

*vi) Kuasa keluaran maksimum, $P_{o(ac)}$.*

*vii) Kecekapan maksimum litar, % $\eta$.*

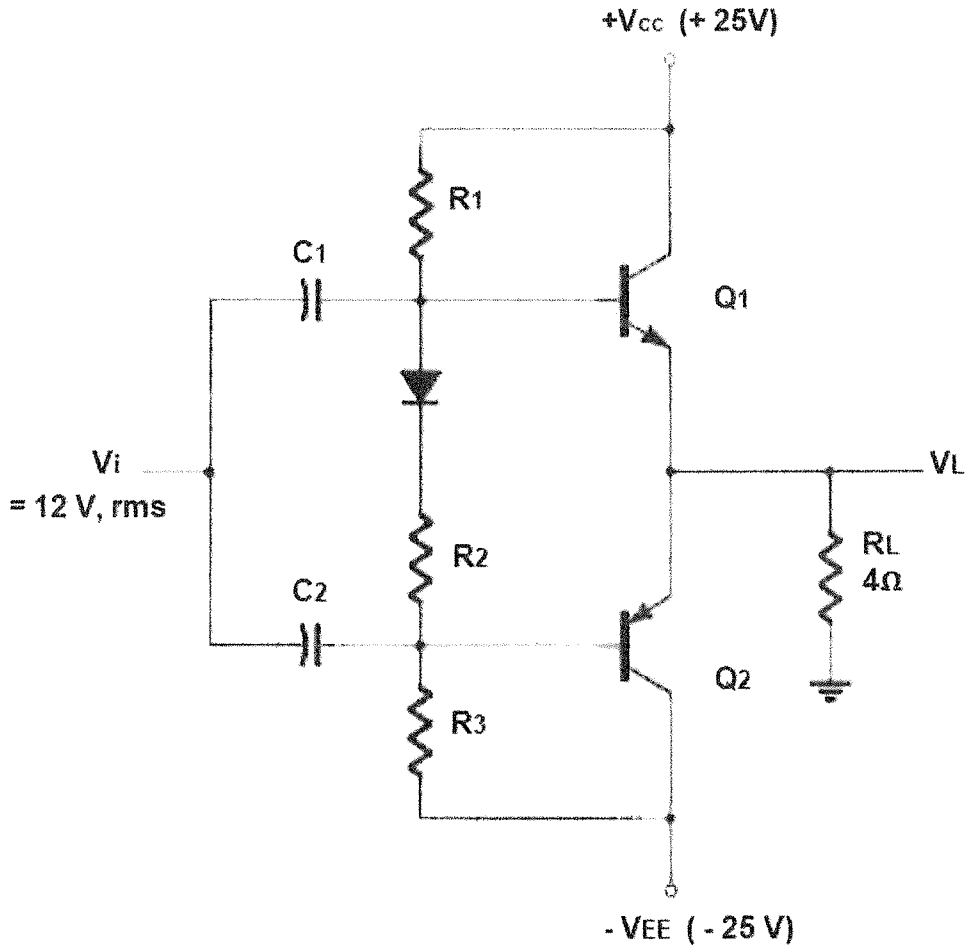


**Figure 4b / *Rajah 4b***

**[100 MARKS / *MARKAH*]**

**END OF QUESTION PAPER/ *KERTAS SOALAN TAMAT***

## *FORMULA*

### JFET / MOSFET FORMULA

$$A_v = A_{v_1}A_{v_2}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Fixed-bias configuration: $V_{GS} = -V_{GG} = V_G$

Self-bias configuration: $V_{GS} = -I_D R_S$

Voltage-divider biasing: $V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$

$$V_{GS} = V_G - I_D R_S$$

Feedback biasing: $V_{DS} = V_{GS}$

$$V_{GS} = V_{DD} - I_D R_D$$

Voltage-divider biasing: $V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$

$$V_{GS} = V_G - I_D R_S$$

$$g_m = y_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$g_m = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

$$r_d = \frac{1}{y_{os}} = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_G = \text{constant}}$$

Table to draw transfer characteristics graph

| $V_{GS}$ | $I_D$ |
|---|---|
| 0 | $I_{DSS}$ |
| $0.3V_P$ | $I_{DSS}/2$ |
| $0.5V_P$ | $I_{DSS}/4$ |
| $V_P$ | 0 mA |

$$G_v = 20\log_{10}\frac{V_o}{V_i}$$

$$P_i(\text{dc}) = V_{CC}I_{CQ}$$

$$P_o(\text{ac}) = V_{CE}(\text{rms})I_C(\text{rms})$$

$$= I_C^2(\text{rms})R_C$$

$$= \frac{V_C^2(\text{rms})}{R_C}$$

$$P_o(\text{ac}) = \frac{V_{CE}(\text{p})I_C(\text{p})}{2}$$

$$= \frac{I_C^2(\text{p})}{2R_C}$$

$$= \frac{V_{CE}^2(\text{p})}{2R_C}$$

$$P_o(\text{ac}) = \frac{V_{CE}(\text{p-p})I_C(\text{p-p})}{8}$$

$$= \frac{I_C^2(\text{p-p})}{8}R_C$$

$$= \frac{V_{CE}^2(\text{p-p})}{8R_C}$$

$$\%\,\eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\%$$

$$I_{\text{dc}} = \frac{2}{\pi}I(\text{p})$$

$$P_i(\text{dc}) = V_{CC}\left(\frac{2}{\pi}I(\text{p})\right)$$

$$P_o(\text{ac}) = \frac{V_L^2(\text{rms})}{R_L}$$

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L}$$

$$\text{maximum } P_i(\text{dc}) = V_{CC}(\text{maximum } I_{\text{dc}})$$

$$V_{CC}\left(\frac{2V_{CC}}{\pi R_L}\right) = \frac{2V_{CC}^2}{\pi R_L}$$

$$\text{maximum } P_{2Q} = \frac{2V_{CC}^2}{\pi^2 R_L}$$

$$r_e = \frac{26\text{ mV}}{I_E}$$

$$Z_i \cong \beta r_e, \qquad Z_o \cong R_C$$

$$A_v = -\frac{R_C}{r_e}, \qquad A_i = -A_v\frac{Z_i}{R_C} \cong \beta$$

Effect of load impedance:

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o}A_{v_{NL}},$$

$$A_{i_L} = \frac{I_o}{I_i} = -A_{v_L}\frac{Z_i}{R_L}$$

Effect of source impedance:

$$V_i = \frac{R_i V_s}{R_i + R_s},$$

$$I_s = \frac{V_s}{R_s + R_i}$$

$$A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s}A_{v_{NL}}$$

Combined effect of load and source Impedance:

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o}A_{v_{NL}},$$

$$A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s}\cdot\frac{R_L}{R_L + R_o}A_{v_{NL}}$$

$$A_{i_L} = \frac{I_o}{I_i} = -A_{v_L}\frac{R_i}{R_L},$$

$$A_{i_s} = \frac{I_o}{I_s} = -A_{v_s}\frac{R_s + R_i}{R_L}$$