UTM UNIVERSITI TEKNOLOGI MALAYSIA

SekolahPendidikanProfesionaldan PendidikanBerterusan (UTMSPACE)

FINAL EXAMINATION / *PEPERIKSAAN AKHIR*
SEMESTER 2 – SESSION 2017 / 2018
PROGRAM KERJASAMA

COURSE CODE *KOD KURSUS*	:	DDWE 1123
COURSE NAME *NAMA KURSUS*	:	DIGITAL ELECTRONICS *ELEKTRONIK DIGITAL*
YEAR / PROGRAMME *TAHUN / PROGRAM*	:	1 DDWE/B/K
DURATION *TEMPOH*	:	2 HOURS 30 MINUTES / *2 JAM 30 MINIT*
DATE *TARIKH*	:	APRIL 2018

INSTRUCTION/*ARAHAN* :

1. ANSWER ALL QUESTIONS.
   JAWAB SEMUA SOALAN .

2. DETACH **PAGES 14** AND **15** AND ATTACH TO YOUR ANSWER BOOKLETS.
   *CERAIKAN **MUKASURAT 14** DAN **15** DAN LAMPIRKAN PADA BUKU JAWAPAN ANDA.*

(You are required to write your name and your lecturer's name on your answer script)
(Pelajar dikehendaki tuliskan nama dan nama pensyarah pada skrip jawapan)

STUDENT'S NAME / *NAMA PELAJAR*	:	.....
I.C NO. / *NO. K/PENGENALAN*	:	.....
YEAR / PROGRAMME *TAHUN / PROGRAM*	:	.....
COLLEGE NAME *NAMA KOLEJ*	:	.....
LECTURER'S NAME *NAMA PENSYARAH*	:	.....

This examination paper consists of **15** pages including the cover
*Kertas soalan ini mengandungi **15** muka surat termasuk kulit hadapan*

PUSAT PROGRAM KERJASAMA

PETIKAN DARIPADA PERATURAN AKADEMIK
ARAHAN AM - PENYELEWENGAN AKADEMIK

1. SALAH LAKU SEMASA PEPERIKSAAN

1.1 Pelajar tidak boleh melakukan mana-mana salah laku peperiksaan seperti berikut :-

1.1.1 memberi dan/atau menerima dan/atau memiliki sebarang maklumat dalam bentuk elektronik, bercetak atau apa jua bentuk lain yang tidak dibenarkan semasa berlangsungnya peperiksaan sama ada di dalam atau di luar Dewan Peperiksaan melainkan dengan kebenaran Ketua Pengawas; atau

1.1.2 menggunakan makluman yang diperolehi seperti di atas bagi tujuan menjawab soalan peperiksaan; atau

1.1.3 menipu atau cuba untuk menipu atau berkelakuan mengikut cara yang boleh ditafsirkan sebagai menipu semasa berlangsungnya peperiksaan; atau

1.1.4 lain-lain salah laku yang ditetapkan oleh Universiti (seperti membuat bising, mengganggu pelajar lain, mengganggu Pengawas menjalankan tugasnya).

2. HUKUMAN SALAH LAKU PEPERIKSAAN

2.1 Sekiranya pelajar didapati telah melakukan pelanggaran mana-mana peraturan peperiksaan ini, setelah diperakukan oleh Jawatankuasa Peperiksaan Fakulti dan disabitkan kesalahannya, Senat boleh mengambil tindakan dari mana-mana satu yang berikut :-

2.1.1 memberi markah SIFAR (0) bagi keseluruhan keputusan peperiksaan kursus yang berkenaan (termasuk kerja kursus); atau

2.1.2 memberi markah SIFAR (0) bagi semua kursus yang didaftarkan pada semester tersebut.

2.2 Jawatankuasa Akademik Fakulti boleh mencadangkan untuk diambil tindakan tatatertib mengikut peruntukan Akta Universiti dan Kolej Universiti, 1971, Kaedah-kaedah Universiti Teknologi Malaysia (Tatatertib Pelajar-pelajar), 1999 bergantung kepada tahap kesalahan yang dilakukan oleh pelajar.

2.3 Pelajar yang didapati melakukan kesalahan kali kedua akan diambil tindakan seperti di perkara 2.1.2 dan dicadang untuk diambil tindakan tatatertib mengikut peruntukan Akta Universiti dan Kolej Universiti, 1971, Kaedah-kaedah Universiti Teknologi Malaysia (Tatatertib Pelajar-pelajar), 1999.

Q1. (a) i. List two (2) advantages of digital techniques over analog.
Senaraikan dua (2) kelebihan teknik digital berbanding analog.

ii. Give a reason why binary system is suitable for implementation in digital system.
Berikan satu sebab mengapa sistem binari sesuai digunakan untuk pelaksanaan dalam sistem digital.

(4 marks/markah)

(b) List the octal numbers in sequence from 166_8 to 201_8.
Senaraikan nombor-nombor oktal dalam turutan dari 166_8 to 201_8.

(3 marks/*markah*)

(c) Convert each of the following decimal number to Gray code and BCD (binary-coded-decimal) code.
Tukarkan setiap nombor desimal berikut kepada kod Gray dan kod BCD.

i. 42

ii. 255

(6 marks/*markah*)

(d) Perform the following addition number in the 2's complement system using eight bits (including the sign bit) for each number. Convert the result back to decimal number.
Laksanakan penambahan nombor desimal berikut dalam sistem pelengkap 2 menggunakan lapan bit (termasuk bit tanda) bagi setiap nombor. Tukar jawapan kembali ke nombor desimal.

i. +17 and -17

ii. -48 and -80

(6 marks/*markah*)

Q2. (a) Refer to Figure Q2(a), simplify the output expression of X by using Boolean Algebra. DeMorgan's Theorem can be used if necessary.

Merujuk kepada Rajah Q2(a), ringkaskan persamaan keluaran bagi X menggunakan Aljabar Boolean. Teorem DeMorgan boleh digunakan jika perlu.

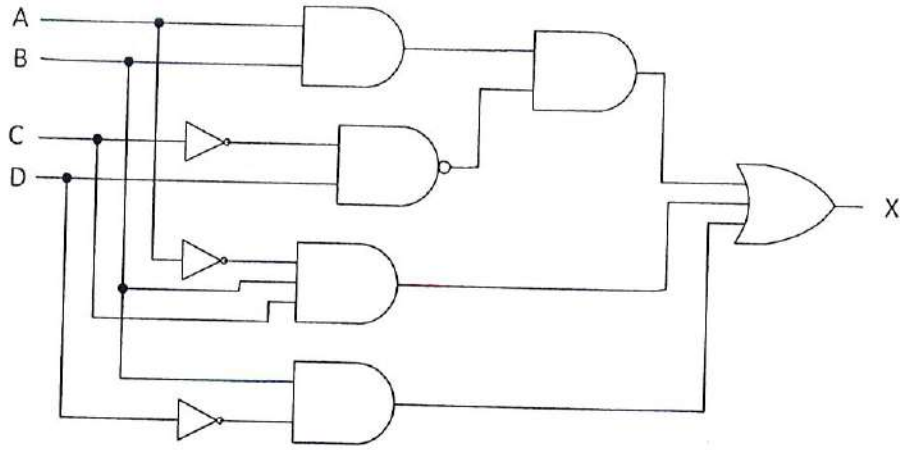


Figure Q2(a) / *Rajah Q2(a)*

(6 marks/*markah*)

(b) Use a Karnaugh map to find minimum SOP (sum-of-product) for each expression:
Gunakan peta Karnaugh untuk dapatkan SOP minimum bagi setiap pernyataan berikut :

i. $Z = \overline{A}\,\overline{B}\,\overline{C} + A\,\overline{B}\,\overline{C} + A\,\overline{B}\,C$

ii. $Y = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + \overline{A}\,BC + A\,\overline{B}\,\overline{C}$

iii. $X = A\,C\,[\,\overline{B}(B + \overline{C}\,)]$

(10 marks/*markah*)

Q3. (a) Design a system which has a single light, L (that can be on or off) that can be controlled by any one of three switches S1, S2 and S3. Switch S1(MSB) is the master on/off switch. If it is down, the lights are off. When the master switch is up, a change in the position of one of the switches (from up to down or down to up) will cause the light to change state.
Rekakan satu sistem yang mempunyai satu lampu, L (yang boleh nyala atau padam) yang boleh dikawal oleh salah satu dari mana-mana suis S1, S2 dan S3. Suis S1 (MSB) adalah suis hidup/mati yang utama. Jika suis utama mati, lampu akan padam. Apabila suis utama hidup, perubahan keadaan bagi salah satu suis (dari hidup ke mati atau mati ke hidup) akan menyebabkan lampu berubah keadaan.

(12 marks/*markah*)

(b) i. Define adders.
Definisikan penambah.

ii. List two (2) types of adder *and draw a block diagram respectively.*
Senaraikan dua (2) jenis penambah dan lukis gambar rajah blok masing-masing.

(5 marks/*markah*)

(c) Refer to Figure Q3(c)(i), write the sequence of digit display on 7-segment by referring to the input waveform in Figure Q3(c)(ii).
Merujuk kepada Rajah Q3(c)(i), Tuliskan jujukan digit yang dipaparkan di paparan 7-ruas dengan merujuk kepada gelombang masukan dalam Rajah Q3(c)(ii).

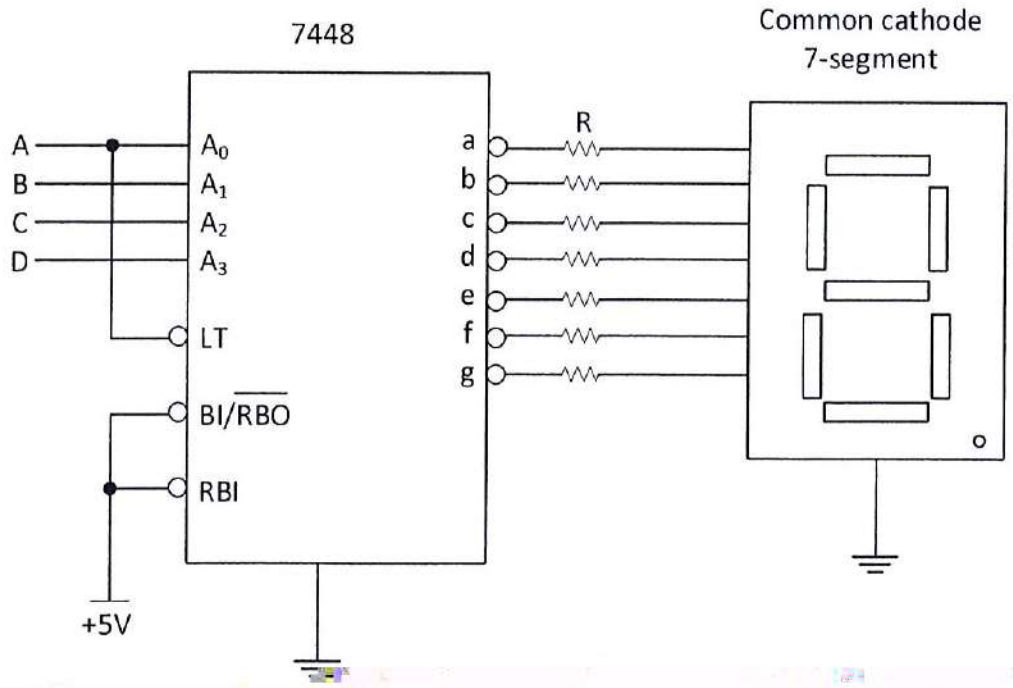


Figure Q3(c)(i) / *Rajah Q3(c)(i)*

7 marks/*markah*)

ing to Figure

npiran dengan
rendah.

Q4. (a) Complete the timing diagram in Figure Q4(a)ii in the attachment by refer
Q4(a)i. Assume the flip- flops are initially low.
Lengkapkan gambar rajah pemasaan di dalam Rajah Q4(a)ii di dalam la
merujuk kepada Rajah Q4(a)i. Anggap keadaan awal bagi flip flop adalal

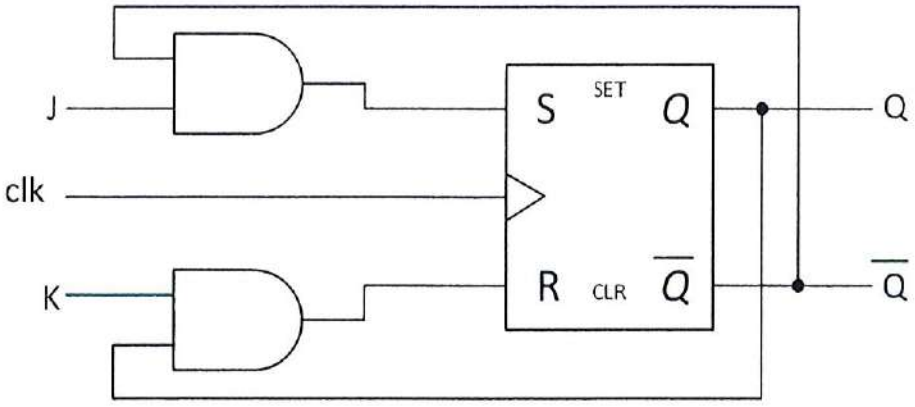


Figure Q4(a)(i) / *Rajah Q4(a)(i)*

(6 marks/*markah*)

(b) The serial in-serial out shift register can be used as a time delay. Give two (2) ways to control the amount of delay.
Daftar anjak bagi masukan sesiri-keluaran sesiri boleh digunakan sebagai lengah masa. Berikan dua (2) cara untuk mengawal jumlah lengah tersebut.

(2 marks/*markah*)

(c) Refer to Figure Q4(c)i;
Rujuk kepada Rajah Q4(c)i;

i. Draw the timing diagram for outputs Q_D, Q_C, Q_B and Q_A in Figure Q4(c)ii in attachment.
Lukiskan gambar rajah pemasaan bagi keluaran Q_D, Q_C, Q_B dan Q_A *di dalam Rajah Q4(c)ii di dalam lampiran.*

ii. What is the counter's modulus?
Apakah mod pembilang tersebut?

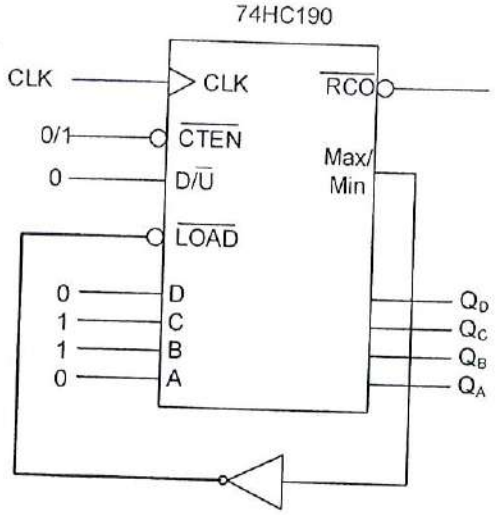


Figure Q4(c)(i) / *Rajah Q4(c)(i)*

(10 marks / *markah*)

Q5. (a) Indicate the term or parameter being described for each of the following statement.
Nyatakan istilah atau parameter yang dihuraikan bagi setiap kenyataan berikut.

i. The total current from the V_{CC} supply when all gate outputs are at LOW level.
Jumlah arus dari bekalan V_{CC} apabila semua keluaran get adalah berparas RENDAH.

ii. The output current that a current sourcing gate provides to a load when the output is at logic HIGH.
Arus keluaran yang dibekalkan oleh get memunca arus kepada get beban pada logik TINGGI.

iii. Current spikes generated by the totem-pole output of a TTL circuit and when both transistors are simultaneously turned on.
Percikan arus dihasilkan oleh keluaran totem-pol bagi litar TTL dan apabila kedua-dua transistor dihidupkan serentak.

iv. Circuit's ability to tolerate noise voltages at its inputs.
Keupayaan litar untuk bertoleransi dengan voltan hingar pada masukan

(8 marks / *markah*)

(b) Refer to datasheet 74ALS20 in Figure Q5(b), determine

Merujuk kepada helaian data 74ALS20 di Rajah Q5(b), tentukan

i. fan out HIGH / *rebak keluar TINGGI*

ii. fan out LOW / *rebak keluar RENDAH*

recommended operating conditions

		SN54ALS20A			SN74ALS20A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8‡			0.8	V
				0.7§				
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

‡ Applies over temperature range −55°C to 70°C
§ Applies over temperature range 70°C to 125°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS20A			SN74ALS20A			UNIT
			MIN	TYP¶	MAX	MIN	TYP¶	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} −2			V_{CC} −2			V
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O#	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		0.22	0.4		0.22	0.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.81	1.5		0.81	1.5	mA

Figure Q5(b) / *Rajah Q5(b)*

(5 marks/*markah*)

(c) Table Q5(c) shows a 74LS series characteristics, calculate the value of:

i) average current.

ii) power dissipation.

iii) speed-power product.

Jadual Q5(c) menunjukkan ciri-ciri siri 74LS, kira nilai:

i) arus purata.

ii) kuasa lesapan.

iii) hasil darab halaju-kuasa.

Table Q5(c) / *Jadual Q5(c)*

Parameter	V_{CC}	V_{OH}	V_{IH}	V_{OL}	V_{IL}	I_{CCH}	I_{CCL}	t_{pd}(avg)
74LS	5.5	2.7	2.0	0.5	0.8	0.85 mA	3 mA	4 ns

(6 marks/*markah*)

(d) Figure Q5(d) is a TTL NAND gate with totem pole output. TTL with totem-pole output has a major problem that the outputs of the two gates cannot be connected together. Give a solution with an aid of diagram of the following TTL NAND gate.
Rajah Q5(d) adalah get TAK DAN bagi TTL dengan keluaran totem-pol. TTL dengan keluaran totem-pol mempunyai masalah utama di mana keluaran bagi kedua-dua get tidak boleh disambungkan bersama. Berikan penyelesaiannya dengan bantuan gambar rajah TTL bagi get TAK DAN tersebut.

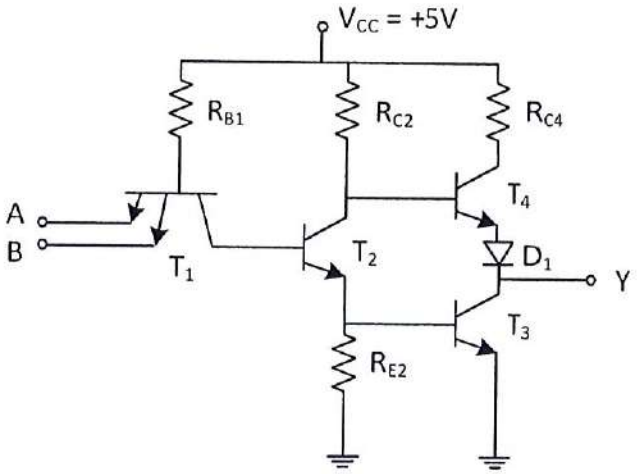


Figure Q5(d) / *Rajah Q5(d)*

(4 marks/ *markah*)

National Semiconductor

January 1992

DM74LS48
BCD to 7-Segment Decoder

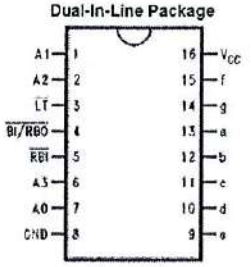
General Description

The 'LS48 translates four lines of BCD (8421) input data into the 7-segment numeral code and provides seven corresponding outputs having pull-up resistors, as opposed to totem pole pull-ups. These outputs can serve as logic signals, with a HIGH output corresponding to a lighted lamp segment, or can provide a 1.3 mA base current to npn lamp driver transistors. Auxiliary inputs provide lamp test, blanking and cascadable zero-suppression functions.

The 'LS48 decodes the input data in the pattern indicated in the Truth Table and the segment identification illustration.

Connection Diagram

Dual-In-Line Package



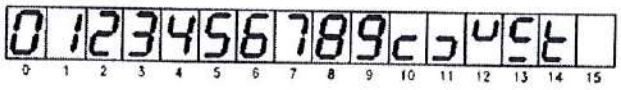
TL/F/10172–1

Order Number DM74LS48M or DM74LS48N
See NS Package Number M16A or N16E

 TL/F/10172

RRD-B30M105/Printed in U. S. A.

Numerical Designations—Resultant Displays



TL/F/10172–4

Truth Table

Decimal Or Function	Inputs						Outputs							
	$\overline{LT}$	$\overline{RBI}$	A_3	A_2	A_1	A_0	$\overline{BI/RBO}$	a	b	c	d	e	f	g
0 (Note 1)	H	H	L	L	L	L	H	H	H	H	H	H	H	L
1 (Note 1)	H	X	L	L	L	H	H	L	H	H	L	L	L	L
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L
$\overline{BI}$ (Note 2)	X	X	X	X	X	X	L	L	L	L	L	L	L	L
$\overline{RBI}$ (Note 3)	H	L	L	L	L	L	L	L	L	L	L	L	L	L
$\overline{LT}$ (Note 4)	L	X	X	X	X	X	H	H	H	H	H	H	H	H

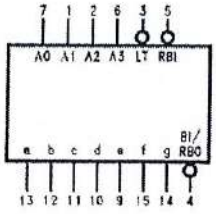
Note 1: $\overline{BI/RBO}$ is wired-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.

Note 2: When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level, regardless of the state of any other input condition.

Note 3: When ripple-blanking input ($\overline{RBI}$) and inputs A_0, A_1, A_2, and A_3 are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a LOW level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

Note 4: When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a HIGH level.

Logic Symbol



TL/F/10172–2

V_{CC} = Pin 16
GND = Pin 8

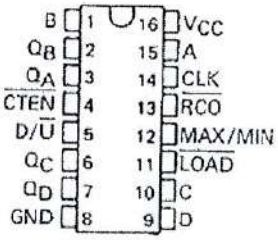
SN54190, SN54191, SN54LS190, SN54LS191, SN74190, SN74191, SN74LS190, SN74LS191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SDLS072 – DECEMBER 1972 – REVISED MARCH 1988

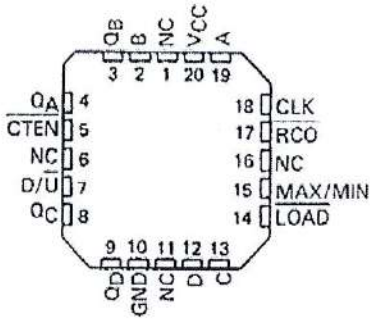
- Counts 8-4-2-1 BCD or Binary
- Single Down/Up Count Control Line
- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presettable with Load Control
- Parallel Outputs
- Cascadable for n-Bit Applications

TYPE	AVERAGE PROPAGATION DELAY	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'190,'191	20ns	25MHz	325mW
'LS190,'LS191	20ns	25MHz	100mW

SN54190, SN54191, SN54LS190, SN54LS191 . . . J PACKAGE
SN74190, SN74191 . . . N PACKAGE
SN74LS190, SN74LS191 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS190, SN54LS191 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

description

The '190, 'LS190, '191, and 'LS191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The '191 and 'LS191 are 4-bit binary counters and the '190 and 'LS190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter count up and when high, it counts down. A false clock may occur if the down/up input changes while the clock is low. A false ripple carry may occur if both the clock and enable are low and the down/up input is high during a load pulse.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

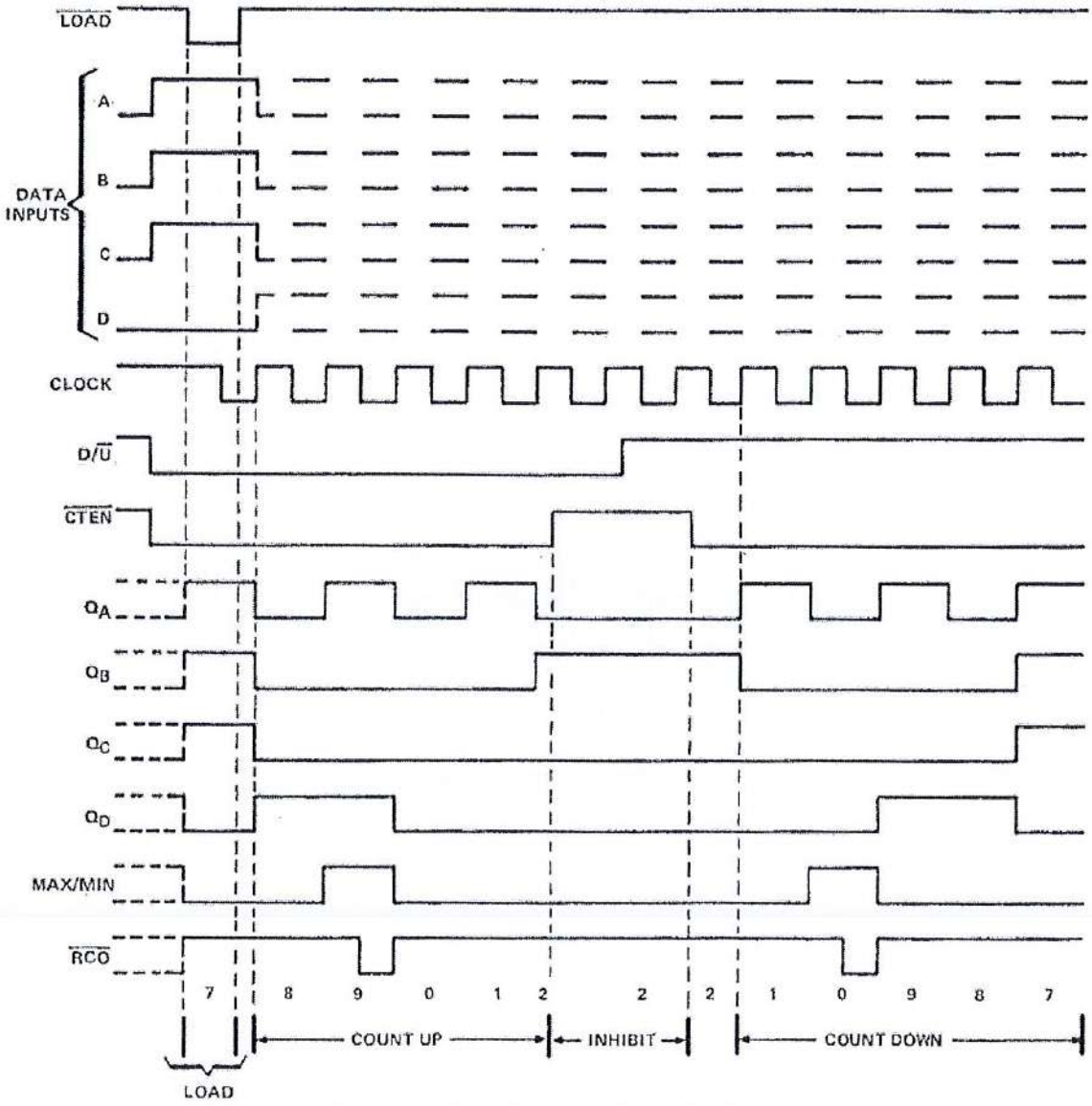
Series 54' and 54LS' are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74' and 74LS' are characterized for operation from 0°C to 70°C.

'190, 'LS190 DECADE COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



Attachment sheet / *Helaian lampiran*

Name:_____

ID Number:_____

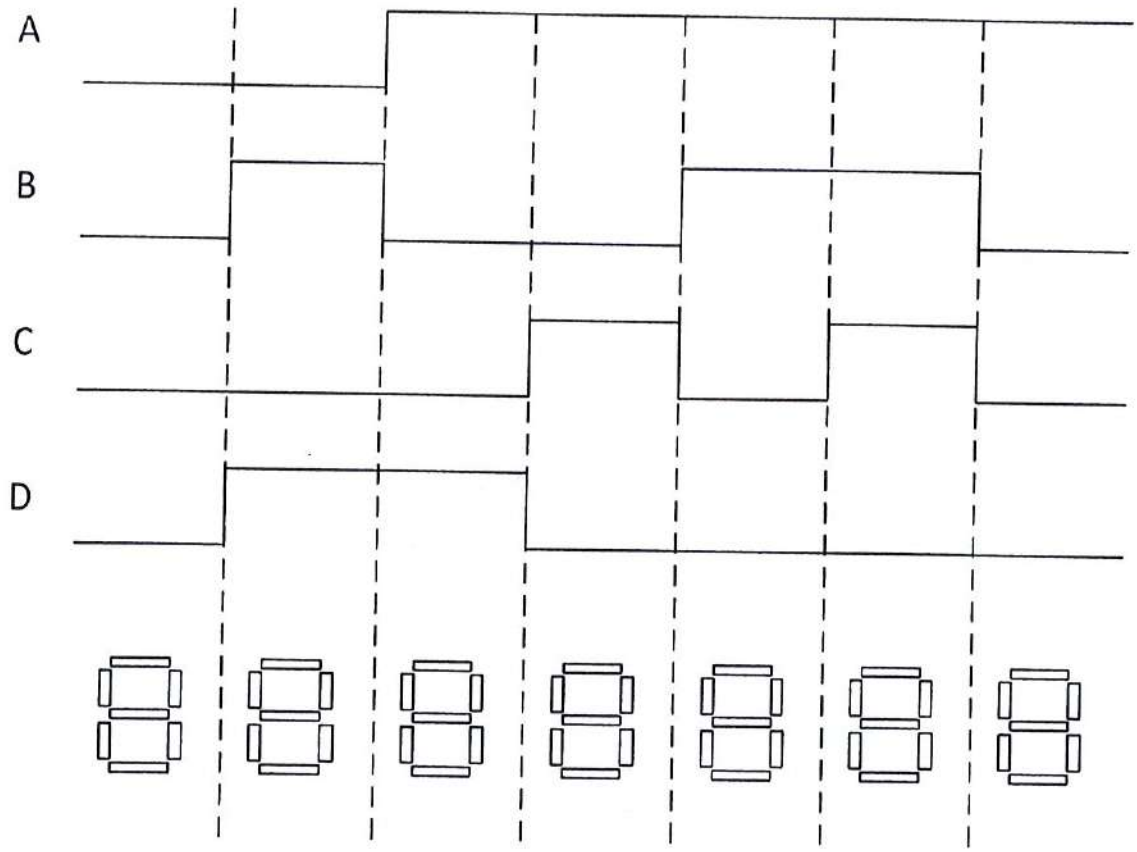


Figure Q3(c)ii / *Rajah Q3(c)ii*

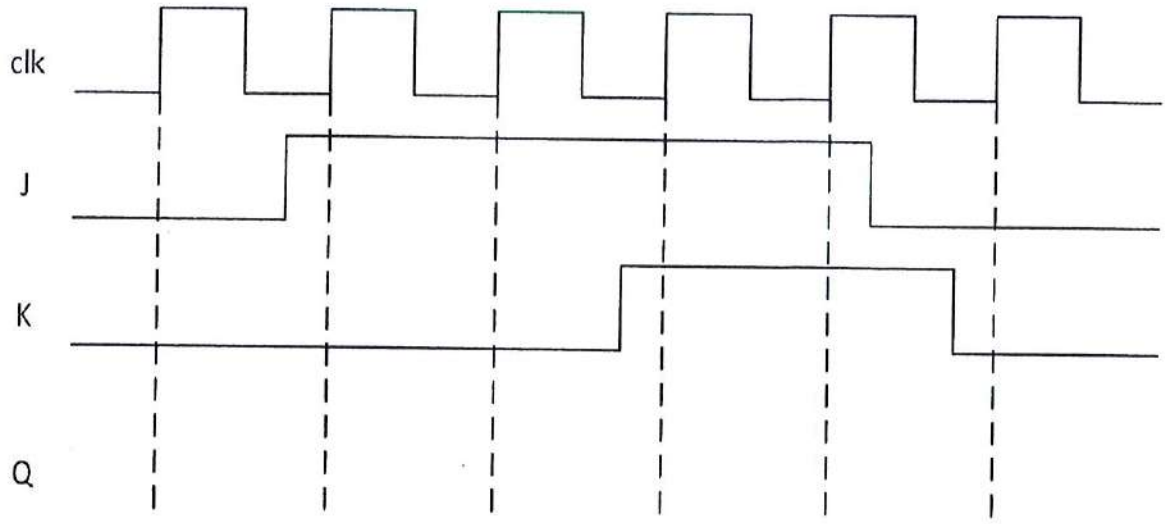


Figure Q4(a)ii / *Rajah Q4(a)ii*

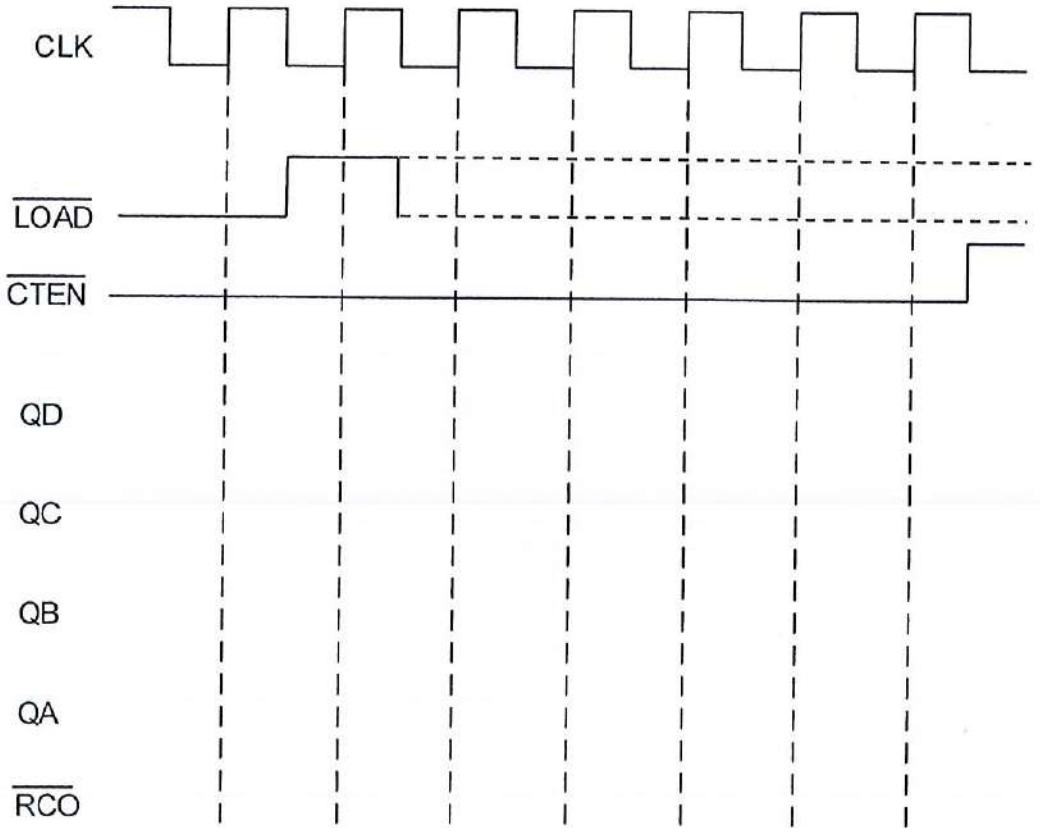


Figure Q4(c)ii / *Rajah Q4(c)ii*

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