UNIVERSITI TEKNOLOGI MALAYSIA

SekolahPendidikanProfesionaldan
PendidikanBerterusan
(UTMSPACE)

FINAL EXAMINATION / *PEPERIKSAAN AKHIR*
SEMESTER 1 – SESSION 2018 / 2019
PROGRAM KERJASAMA

COURSE CODE *KOD KURSUS*	:	DDWE 1123
COURSE NAME *NAMA KURSUS*	:	DIGITAL ELECTRONICS` *ELEKTRONIK DIGITAL*
YEAR / PROGRAMME *TAHUN / PROGRAM*	:	1 DDWE/B/K
DURATION *TEMPOH*	:	2 HOURS 30 MINUTES / *2 JAM 30 MINIT*
DATE *TARIKH*	:	NOV 2018

INSTRUCTION/*ARAHAN* :

1. ANSWER ALL QUESTIONS.
   JAWAB SEMUA SOALAN .

2. DETACH **PAGES 14** AND **15** AND ATTACH TO YOUR ANSWER BOOKLETS.
   *CERAIKAN **MUKASURAT 14** DAN **15** DAN LAMPIRKAN PADA BUKU JAWAPAN ANDA.*

(You are required to write your name and your lecturer's name on your answer script)
(Pelajar dikehendaki tuliskan nama dan nama pensyarah pada skrip jawapan)

STUDENT'S NAME / *NAMA PELAJAR*	:	.....
I.C NO. / *NO. K/PENGENALAN*	:	.....
YEAR / PROGRAMME *TAHUN / PROGRAM*	:	.....
COLLEGE NAME *NAMA KOLEJ*	:	.....
LECTURER'S NAME *NAMA PENSYARAH*	:	.....

This examination paper consists of **15** pages including the cover
*Kertas soalan ini mengandungi **15** muka surat termasuk kulit hadapan*

PUSAT PROGRAM KERJASAMA

PETIKAN DARIPADA PERATURAN AKADEMIK
ARAHAN AM - PENYELEWENGAN AKADEMIK

1. SALAH LAKU SEMASA PEPERIKSAAN

1.1 Pelajar tidak boleh melakukan mana-mana salah laku peperiksaan seperti berikut :-

1.1.1 memberi dan/atau menerima dan/atau memiliki sebarang maklumat dalam bentuk elektronik, bercetak atau apa jua bentuk lain yang tidak dibenarkan semasa berlangsungnya peperiksaan sama ada di dalam atau di luar Dewan Peperiksaan melainkan dengan kebenaran Ketua Pengawas; atau

1.1.2 menggunakan makluman yang diperolehi seperti di atas bagi tujuan menjawab soalan peperiksaan; atau

1.1.3 menipu atau cuba untuk menipu atau berkelakuan mengikut cara yang boleh ditafsirkan sebagai menipu semasa berlangsungnya peperiksaan; atau

1.1.4 lain-lain salah laku yang ditetapkan oleh Universiti (seperti membuat bising, mengganggu pelajar lain, mengganggu Pengawas menjalankan tugasnya).

2. HUKUMAN SALAH LAKU PEPERIKSAAN

2.1 Sekiranya pelajar didapati telah melakukan pelanggaran mana-mana peraturan peperiksaan ini, setelah diperakukan oleh Jawatankuasa Peperiksaan Fakulti dan disabitkan kesalahannya, Senat boleh mengambil tindakan dari mana-mana satu yang berikut :-

2.1.1 memberi markah SIFAR (0) bagi keseluruhan keputusan peperiksaan kursus yang berkenaan (termasuk kerja kursus); atau

2.1.2 memberi markah SIFAR (0) bagi semua kursus yang didaftarkan pada semester tersebut.

2.2 Jawatankuasa Akademik Fakulti boleh mencadangkan untuk diambil tindakan tatatertib mengikut peruntukan Akta Universiti dan Kolej Universiti, 1971, Kaedah-kaedah Universiti Teknologi Malaysia (Tatatertib Pelajar-pelajar), 1999 bergantung kepada tahap kesalahan yang dilakukan oleh pelajar.

2.3 Pelajar yang didapati melakukan kesalahan kali kedua akan diambil tindakan seperti di perkara 2.1.2 dan dicadang untuk diambil tindakan tatatertib mengikut peruntukan Akta Universiti dan Kolej Universiti, 1971, Kaedah-kaedah Universiti Teknologi Malaysia (Tatatertib Pelajar-pelajar), 1999.

Q1. (a) i. Data sampling is one of the factors that influence the efficiency of digital system. Explain briefly the concept of data sampling in consideration of digital representation and data resolution.
Pensampelan data adalah salah satu faktor yang mempengaruhi kecekapan sistem digital. Terangkan dengan ringkas konsep pensampelan data sebagai pertimbangan digital perwakilan dan resolusi data.

ii. Which of the following involve analog quantities and which involve digital quantities?
Yang manakah melibatkan kuantiti analog dan yang melibatkan digital kuantiti?
a. volume of water in a bucket
jumlah air dalam baldi
b. height of child measured by putting a mark on the wall.
ketinggian anak diukur dengan meletakkan tanda di dinding
c. timer setting on a microwave oven.
tetapan pemasa pada ketuhar gelombang mikro.

(5 marks/markah)

(b) Convert each of the following to Gray code.
Tukarkan setiap ysng berikut kepada kod Gray.
i. $01100111_{BCD8421}$
ii. $1A1_{16}$
iii. 67_8

(8 marks/*markah*)

(c) Perform the following addition number in the 2's complement system using six bits (including the sign bit) for each number and state whether overflow occur or not. Convert the result back to decimal number.
Laksanakan penambahan nombor desimal berikut dalam sistem pelengkap 2 menggunakan enam bit (termasuk bit tanda) bagi setiap nombor dan nyatakan sama ada berlaku limpahan atau tidak. Tukar jawapan kembali ke nombor desimal.
i. $-4_{10} - 30_{10}$
ii. $-4_{10} + 13_{10}$

(6 marks/*markah*)

Q2. (a) Figure Q2(a) shows a digital circuit where the boxes represent the logic gates. Sketch the appropriate gates in the given boxes correspond to the following statement. [*The result of the first statement is shown for reference.*

Rajah Q2 (a) menunjukkan litar digital di mana kotak mewakili pintu logik. Lakarkan pintu yang sesuai di dalam kotak yang diberikan sesuai dengan pernyataan berikut. [Hasil pernyataan pertama ditunjukkan untuk rujukan.]

- V will be HIGH only when A is LOW.
  V akan menjadi TINGGI sahaja apabila A adalah RENDAH.
- W will be HIGH when either B or C is LOW where B is not equal to C.
  W akan TINGGI apabila B atau C adalah RENDAH di mana B adalah tidak sama dengan C.
- X will be HIGH when both D and E are either LOW or HIGH.
  X akan menjadi TINGGI apabila kedua-dua D dan E sama ada RENDAH atau TINGGI.
- Y will be HIGH when either W or X is HIGH.
  Y akan menjadi TINGGI apabila W atau X adalah TINGGI.
- Z will go LOW only when V and Y are HIGH.
  Z akan menjadi RENDAH sahaja apabila V dan Y adalah TINGGI.

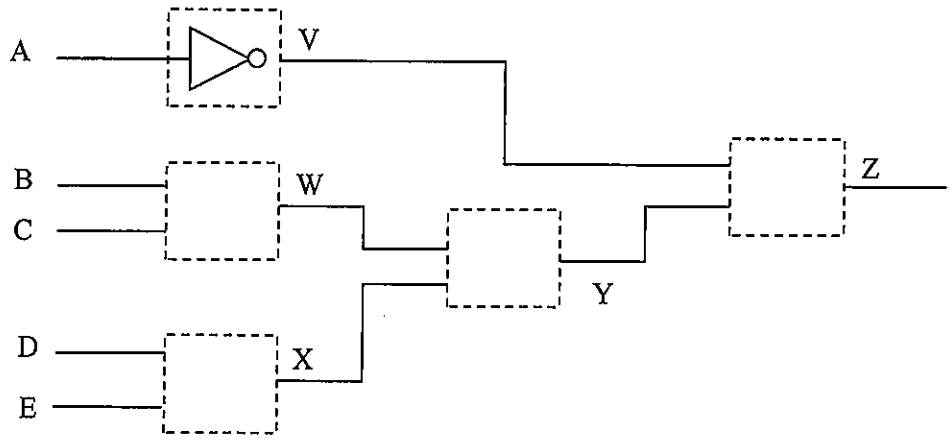


Figure Q2(a)/ *Rajah Q2(a)*

(8 marks/*markah*)

(b) Use a Karnaugh map to find minimum SOP (sum-of-product) for each expression:
Gunakan peta Karnaugh untuk dapatkan SOP minimum bagi setiap pernyataan berikut :

i. $Z = (A\bar{B}\,(C + BD) + \bar{A}\,\bar{B}\,)\,C$

ii. $Y = AC\,(\,\bar{B} + C\,) + A\,B\,\bar{D} + B\,\bar{D}$

iii. $X = A\,C\,[\,\bar{B}(B + \bar{C}\,)]$

(9 marks/*markah*)

Q3. (a) Before leaving port, the loading bay controller and captain of a Car Ferry carry out pre-departure safety checks. When all checks have been completed they each move a switch from the down to the up position.

- When both switches are down, a red indicator(R) on the instrument panel is on.
- When any one of the switches, is in the up position, the indicator light changes to yellow (Y).
- When both switches are in the up position, a green indicator (G) comes on.
- The engines of the Car Ferry can only be started when the green indicator (G) is on.

Assume that the switches provide logic level 0 in the up position and logic level 1 in their down position. The LED indicators operate on logic level 1.

Sebelum meninggalkan pelabuhan, pengawal bay pemuatan dan kapten kereta Ferry menjalankan pemeriksaan keselamatan pra-berlepas. Apabila semua pemeriksaan telah selesai, mereka masing-masing memindahkan suis dari bawah ke kedudukan atas.

- *Apabila kedua-dua suis turun, penunjuk merah (R) pada panel instrumen dihidupkan.*
- *Apabila mana-mana suis, berada di kedudukan atas, lampu indikator berubah menjadi kuning (Y).*
- *Apabila kedua-dua suis berada di kedudukan atas, penunjuk hijau (G) muncul.*
- *Enjin Kereta Feri hanya boleh dimulakan apabila penunjuk hijau (G) dihidupkan.*

Anggapkan bahawa suis memberikan tahap logik 0 dalam kedudukan naik dan tahap logik 1 dalam kedudukan bawah mereka. Penunjuk LED beroperasi pada tahap logik 1

i) Complete the following truth table for the system in Figure Q3(a) in the attachment.
Lengkapkan jadual benar bagi sistem di Rajah Q3(a) di dalam lampiran

ii) Write down a Boolean expression for **R, Y** and **G**.
*Tuliskan persamaan Boolean bagi **R, Y** dan **G**.*

iii) Draw the circuit for the following system.
Lukiskan litar bagi sistem tersebut

(15 marks/*markah*)

(b) Referring to Figure Q3(b), the 74138 decoder has an input signal of A_0, A_1 and A_2. Determine the input for binary code that can activate the output devices at $\overline{O_0}$, $\overline{O_3}$, $\overline{O_5}$, $\overline{O_6}$ and $\overline{O_7}$ in Table Q3(b) in attachment. Refer the data sheet in appendix.

Merujuk Rajah Q3(b), IC penyahkod 74138 mempunyai isyarat masukan A_0, A_1 dan A_2. Tentukan kod binari bagi masukan yang boleh mengaktifkan peranti-peranti pada $\overline{O_0}$, $\overline{O_3}$, $\overline{O_5}$, $\overline{O_6}$ dan $\overline{O_7}$ dalam Jadual Q3(b) di dalam lampiran. Rujuk helaian data di dalam lampiran.

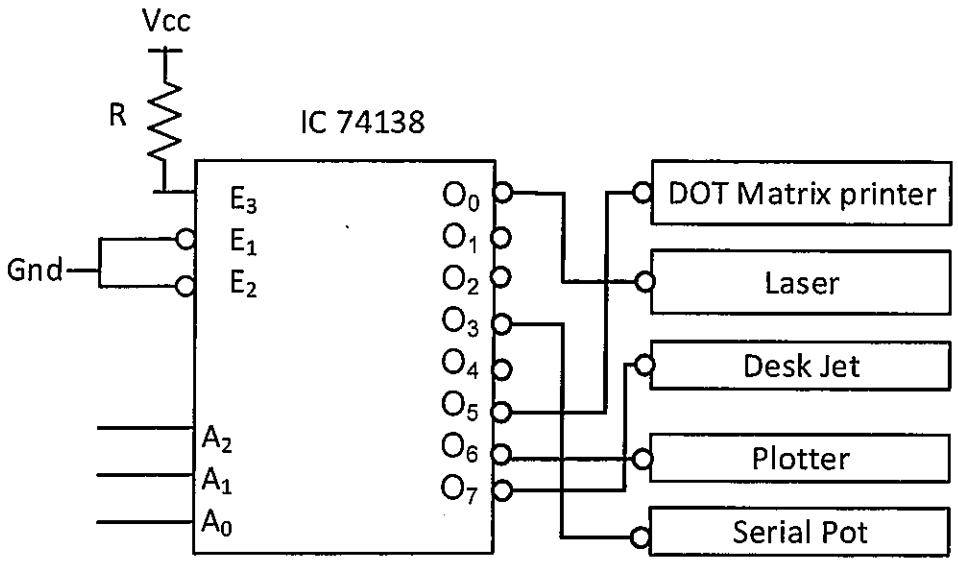


Figure Q3(b) / *Rajah Q3(b)*

(10 marks/*markah*)

Q4. (a) Refer to the Figure Q4(a)(i), complete the timing diagram of Q and Y in Figure Q4(a)(ii) in attachment sheet. Assume the initial condition of Q is LOW.

Merujuk Rajah Q4(a)i, lengkapkan rajah pemasaan bagi Q dan Y pada Rajah Q4(a)ii di dalam helaian lampiran. Anggap keadaan awal bagi Q adalah RENDAH.

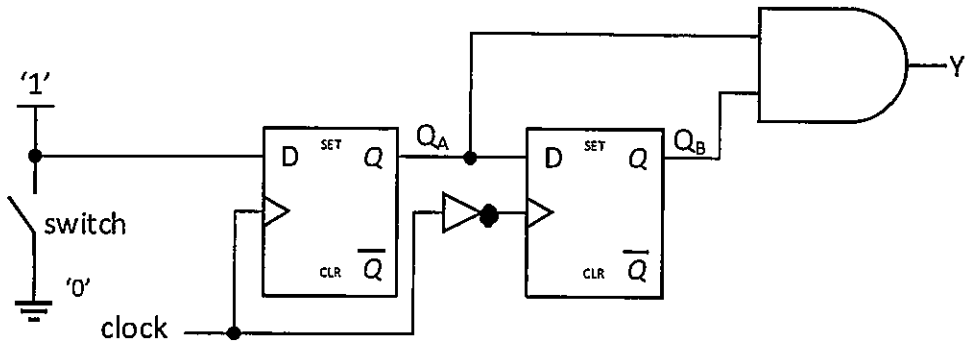


Figure Q4(a)(i) / *Rajah Q4(a)(i)*

(6 marks/*markah*)

(b) Complete the circuit diagram in Figure Q4(b) in the attachment to make a 4-bit Serial-In-Parallel-Out shift register. Label the outputs A, B, C and D.
Lengkapkan gambar rajah litar dalam Rajah Q4(b) di dalam lampiran untuk hasilkan 4-bit Masukan-Sesiri-Keluaran-Selari daftar anjak. Labelkan keluaran-keluaran A, B, C dan D.

(6 marks/*markah*)

(c) Refer to Figure Q4(c)i;
Rujuk kepada Rajah Q4(c)i;

i. What is the counter's modulus?
Apakah mod pembilang tersebut?

ii. Briefly explain what happen to the output if LOAD is LOW.
Terangkan secara ringkas apa yang berlaku pada keluaran jika masukan LOAD adalah RENDAH.

iii. What logic level must be present on the control inputs of $\overline{\text{LOAD}}$, $\overline{\text{CTEN}}$ and D/$\overline{\text{U}}$ in order for the 74HC190 to count down with pulses that appear on the CLK?
Tahap logik apa yang harus ada pada kawalan masukan bagi $\overline{LOAD}$, $\overline{CTEN}$ dan D/$\overline{U}$ agar 74HC190 membilang menurun dengan denyutan hadir pada CLK?

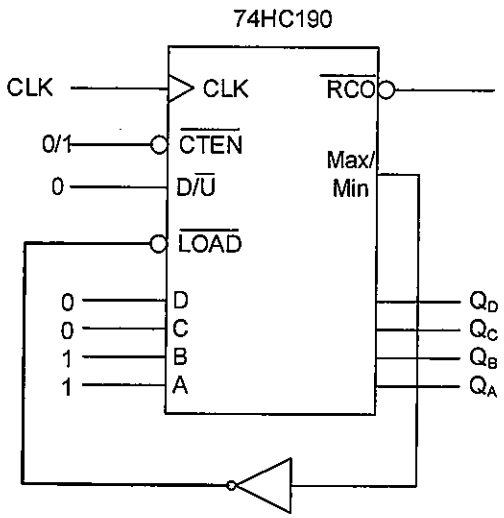


Figure Q4(c)(i) / *Rajah Q4(c)(i)*

(8 marks / *markah*)

Q5. (a) What are the parameters to be considered in determining the number of gates or loads of one family that can be driven from an output of another family?
Apakah parameter yang perlu diambil kira untuk menentukan bilangan get atau beban daripada satu famili yang boleh dipacu daripada keluaran family yang lain?

(4 marks/ *markah*)

(b) Refer to Table Q5(b) in an attachment calculate and compare the power dissipation of a 7400 versus a 74LS00 by using total supply current, I_{CCL} and I_{CCH}.
Dengan merujuk kepada Jadual Q5(b) di dalam lampiran , kira dan bandingkan kuasa lesapan di antara 7400 dan 74LS00 dengan menggunakan jumlah arus bekalan, I_{CCL} dan I_{CCH}.

(6 marks/ *markah*)

(c) Determine the average propagation delay of NAND gate 74ALS00 if t_{PLH} = 15 ns and t_{PHL} = 9 ns.
Tentukan purata lengah perambatan bagi get TAK-DAN 74ALS00 jika t_{PLH} = 15ns dan t_{PHL} = 9 ns.

(6 marks/*markah*)

(d) List three (3) methods to handle the unused input of TTL.
Senaraikan tiga (3) cara untuk mengendalikan masukan yang tidak digunakan bagi TTL.

(3 marks/ *markah*)

MOTOROLA

1-OF-8 DECODER/ DEMULTIPLEXER

SN54/74LS138

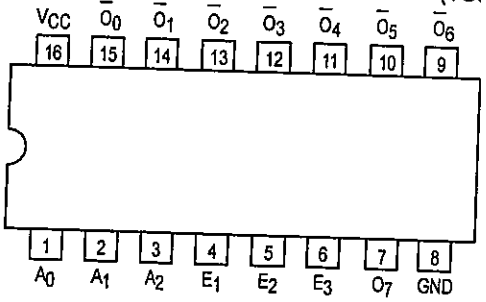
1-OF-8 DECODER/ DEMULTIPLEXER

LOW POWER SCHOTTKY

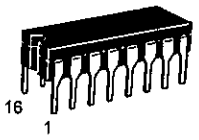
The LSTTL/MSI SN54/74LS138 is a high speed 1-of-8 Decoder/ Demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LS138 devices or to a 1-of-32 decoder using four LS138s and one inverter. The LS138 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Demultiplexing Capability
- Multiple Input Enable for Easy Expansion
- Typical Power Dissipation of 32 mW
- Active Low Mutually Exclusive Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

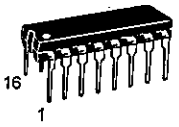
CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

PIN NAMES

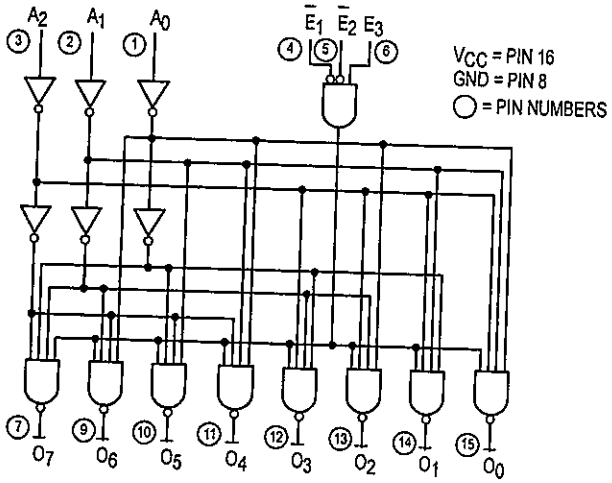
		LOADING (Note a) HIGH	LOW
$\overline{A}_0$–$\overline{A}_2$	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_1$, $\overline{E}_2$	Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
E_3	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0$–$\overline{O}_7$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

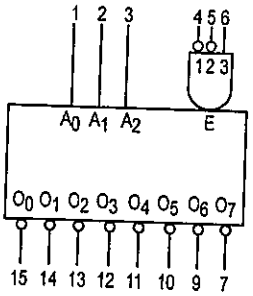
ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC DIAGRAM



LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

SN54/74LS138

FUNCTIONAL DESCRIPTION

The LS138 is a high speed 1-of-8 Decoder/Demultiplexer fabricated with the low power Schottky barrier diode process. The decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled provides eight mutually exclusive active LOW Outputs ($\overline{O}_0 - \overline{O}_7$). The LS138 features three Enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LS138s and one inverter. (See Figure a.)

The LS138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

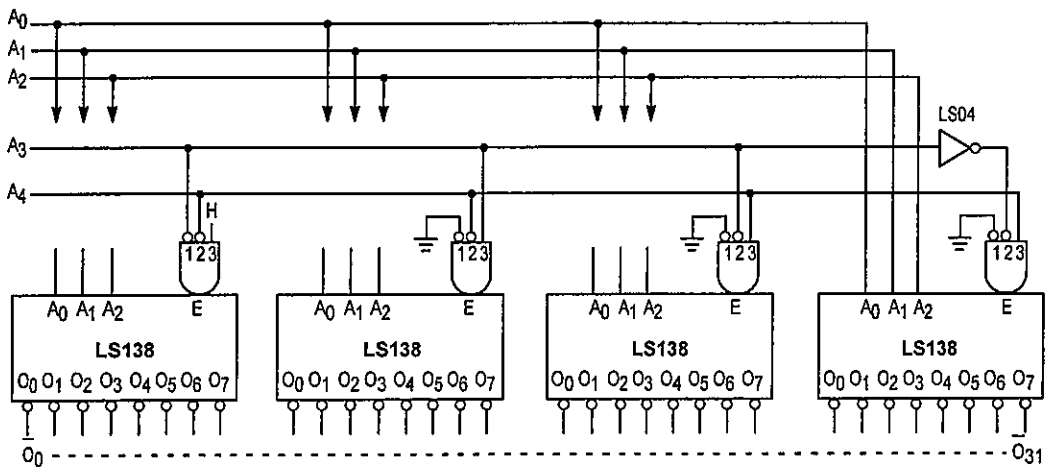


Figure a

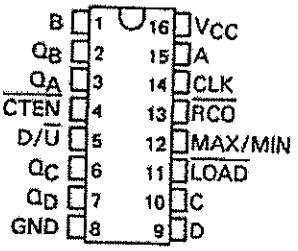
SN54190, SN54191, SN54LS190, SN54LS191, SN74190, SN74191, SN74LS190, SN74LS191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SDLS072 – DECEMBER 1972 – REVISED MARCH 1988

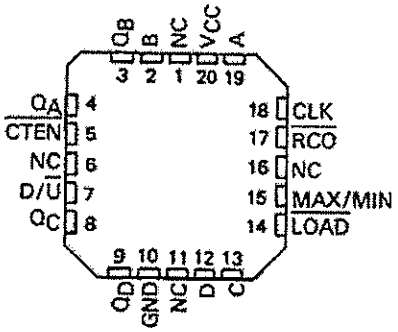
- Counts 8-4-2-1 BCD or Binary
- Single Down/Up Count Control Line
- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presettable with Load Control
- Parallel Outputs
- Cascadable for n-Bit Applications

TYPE	AVERAGE PROPAGATION DELAY	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'190,'191	20ns	25MHz	325mW
'LS190,'LS191	20ns	25MHz	100mW

SN54190, SN54191, SN54LS190, SN54LS191 . . . J PACKAGE
SN74190, SN74191 . . . N PACKAGE
SN74LS190, SN74LS191 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS190, SN54LS191 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

description

The '190, 'LS190, '191, and 'LS191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The '191 and 'LS191 are 4-bit binary counters and the '190 and 'LS190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter count up and when high, it counts down. A false clock may occur if the down/up input changes while the clock is low. A false ripple carry may occur if both the clock and enable are low and the down/up input is high during a load pulse.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Series 54' and 54LS' are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74' and 74LS' are characterized for operation from 0°C to 70°C.

'190, 'LS190 DECADE COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.

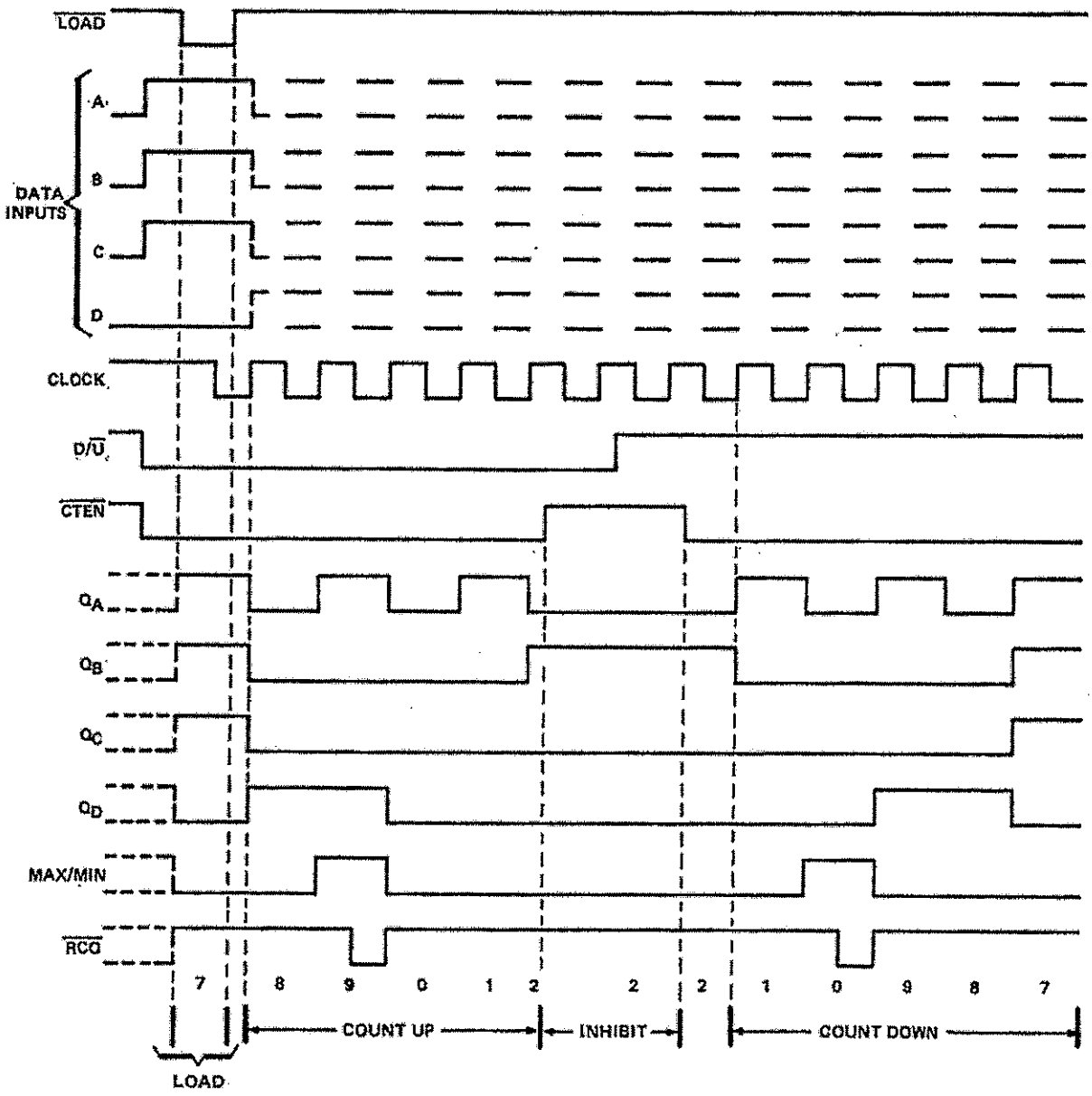


Table Q5(b) / *Jadual Q5(b)*

	CMOS					TTL			
Parameter	**4001B**	**74HC**	**74HCT**	**74AC**	**74ACT**	**74**	**74LS**	**74AS**	**74ALS**
$V_{IH(min)}$	3.5	3.5	2.0	3.5	2.0	2.0	2.0	2.0	2.0
$V_{IL(max)}$	1.5	1.0	0.8	1.5	0.8	0.8	0.8	0.8	0.8
$V_{OH(min)}$	4.95	4.9	4.9	4.9	4.9	2.4	2.7	2.7	2.7
$V_{OL(max)}$	0.05	0.1	0.1	0.1	0.1	0.4	0.5	0.5	0.4
$I_{IH(min)}$	1 uA	1 uA	1 uA	1 uA	1 uA	40 uA	20 uA	200 uA	20 uA
$I_{IL(max)}$	1 uA	1 uA	1 uA	1 uA	1 uA	1.6 mA	0.4 mA	2 mA	100 uA
$I_{OH(min)}$	0.4 mA	4 mA	4 mA	24 mA	24 mA	0.4 mA	0.4 mA	2 mA	400 uA
$I_{OL(max)}$	0.4 mA	4 mA	4 mA	24 mA	24 mA	16 mA	8 mA	20 mA	8 mA
I_{CCL}						4 mA	0.8 mA		
I_{CCH}						12 mA	2.4 mA		
Propagation delay						10 ns	9 ns		

Attachment sheet / *Helaian lampiran*

Name:_____

ID Number:_____

Table Q3(a)i / *Jadual Q3(a)i*

Inputs		**Outputs**		
A	**B**	**R**	**Y**	**G**
0	0			
0	1			
1	0			
1	1			

Table Q3(b) / *Jadual Q3(b)*

A_2	A_1	A_0	Output
			Dot Matrix printer
			Laser
			Desk Jet
			Plotter
			Serial Port

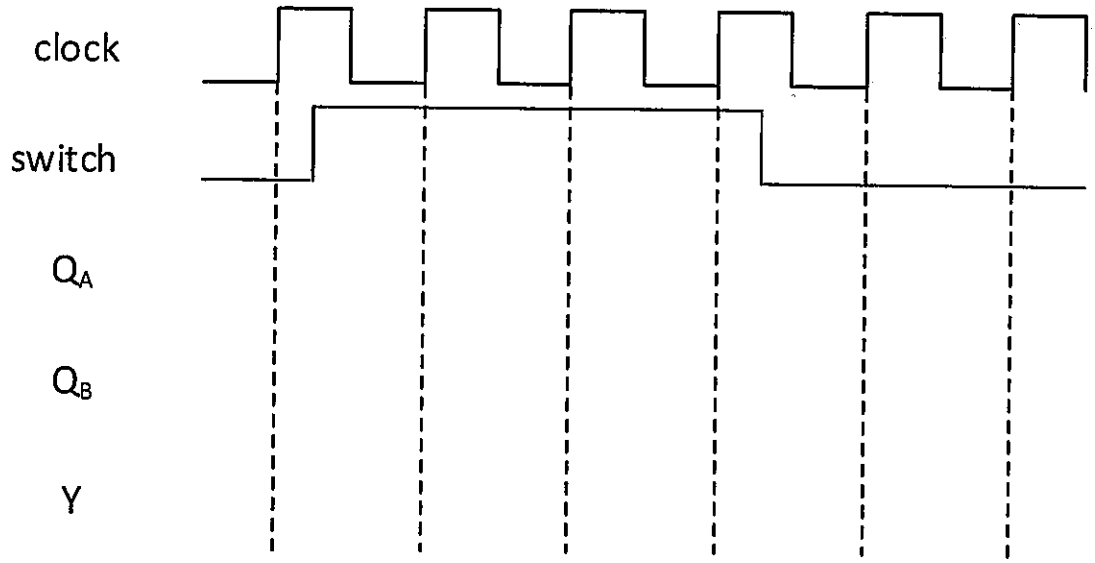


Figure Q4(a)ii / *Rajah Q4(a)ii*

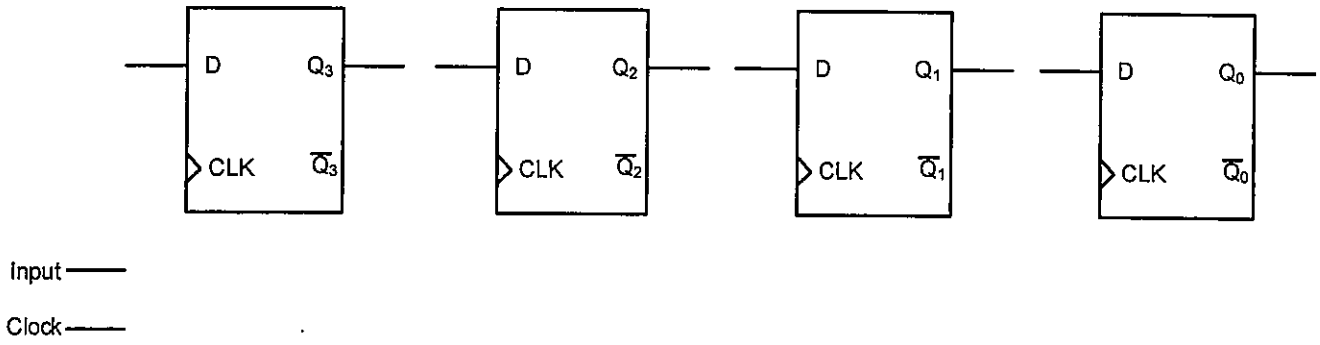


Figure Q4(b) / *Rajah Q4(b)*

Mukasurat ini sengaja dibiarkan kosong

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