UTM UNIVERSITI TEKNOLOGI MALAYSIA

Sekolah Pendidikan Profesional dan Pendidikan Berterusan (UTMSPACE)

FINAL EXAMINATION / *PEPERIKSAAN AKHIR*
SEMESTER 2 – SESSION 2016 / 2017
PROGRAM KERJASAMA

COURSE CODE *KOD KURSUS*	:	DDWE 1123
COURSE NAME *NAMA KURSUS*	:	DIGITAL ELECTRONIC / *ELEKTRONIK DIGITAL*
YEAR / PROGRAMME *TAHUN / PROGRAM*	:	1 / DDWE / K / B
DURATION *TEMPOH*	:	2 HOURS 30 MINUTES / *2 JAM 30 MINIT*
DATE *TARIKH*	:	MAC / APRIL 2017

INSTRUCTION/*ARAHAN* :

1. Answer ALL questions.
   Jawab SEMUA soalan.

2. Detach pages 13 and 14 and attach to your answer booklets .
   Ceraikan mukasurat 13 dan 14 dan lampirkan pada buku jawapan anda.

(You are required to write your name and your lecturer's name on your answer script)
(Pelajar dikehendaki tuliskan nama dan nama pensyarah pada skrip jawapan)

NAME / *NAMA*	:	.....
I.C NO. / *NO. K/PENGENALAN*	:	.....
YEAR / COURSE *TAHUN / KURSUS*	:	.....
COLLEGE NAME *NAMA KOLEJ*	:	.....
LECTURER'S NAME *NAMA PENSYARAH*	:	.....

This examination paper consists of **14** pages including the cover
Kertas soalan ini mengandungi **14** *muka surat termasuk kulit hadapan*

PUSAT PENGAJIAN DIPLOMA
SPACE
UTM *International Campus*
PETIKAN DARIPADA PERATURAN AKADEMIK

ARAHAN AM

1. PENYELEWENGAN AKADEMIK (SALAH LAKU PEPERIKSAAN)

1.1 Pelajar tidak boleh melakukan mana-mana salah laku peperiksaan seperti berikut:-

(a) Memberi atau menerima atau memiliki sebarang maklumat dalam bentuk elektronik, cetak atau apa-apa jua bentuk lain yang ada kaitan dengan sesuatu kursus semasa peperiksaan bagi kursus tersebut dijalankan sama ada di dalam atau di luar Dewan/Bilik Peperiksaan melainkan dengan kebenaran Ketua Pengawas.

(b) Menggunakan maklumat yang diperolehi seperti di perkara 1(a) di atas bagi tujuan menjawab soalan peperiksaan.

(c) Menipu atau cuba untuk menipu atau berkelakuan mengikut cara yang boleh ditafsirkan sebagai menipu atau cuba untuk menipu semasa peperiksaan sedang berjalan.

(d) Lain-lain salah laku yang ditetapkan oleh Universiti.

2. HUKUMAN

2.1 Sekiranya pelajar didapati telah melakukan pelanggaran mana-mana peraturan peperiksaan ini, setelah dibicara oleh Jawatankuasa Akademik Fakulti dan disabitkan kesalahannya, Senat boleh mengambil tindakan dari mana-mana satu, atau kombinasi yang sesuai dari dua atau lebih hukuman-hukuman berikut :-

(a) Memberi markah SIFAR (0) bagi keseluruhan keputusan peperiksaan mata pelajaran yang berkenaan. (Termasuk kerja kursus).

(b) Memberi markah SIFAR (0) bagi semua mata pelajaran yang didaftarkan kepada semester tersebut.

(c) Pelajar yang didapati melakukan kesalahan kali kedua hendaklah diambil tindakan tatatertib mengikut peruntukan Akta Universiti dan Kolej Universiti, 1971, Kaedah-kaedah Universiti Teknologi Malaysia (Tatatertib Pelajar-pelajar), 1999.

☆☆☆☆☆☆☆☆☆☆☆☆☆☆☆

Q1. (a) Perform the conversion:
Laksanakan penukaran:

i) 102_{10} to binary
ii) 452_8 to hexadecimal
iii) 1101010_{Gray} to binary

(6 marks / markah)

(b) Perform a BCD addition for the following decimal numbers.
Laksanakan operasi penambahan BCD bagi nombor perpuluhan berikut.

i) 25_{10} and 13_{10}
ii) 135_{10} and 296_{10}

(6 marks / markah)

(c) Write the output expression for each circuit in Figure Q1(c).
Tuliskan persamaan keluaran bagi setiap litar dalam Rajah Q1(c).

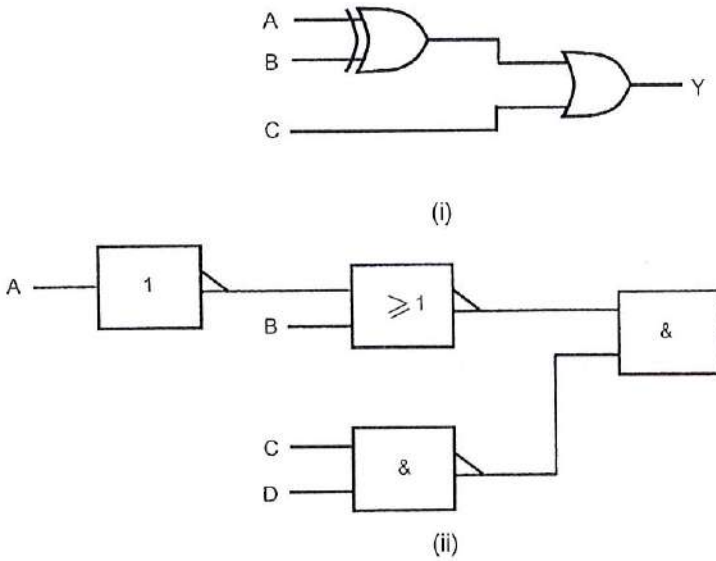


Figure Q1(c) / *Rajah Q1(c)*

(4 marks / *markah*)

Q2. (a) Simplify the following expression using Boolean algebra.
Ringkaskan persamaan-persamaan berikut menggunakan aljabar Boolean.

i) $X = AB + A\overline{BC} + \overline{\overline{B}D}$

ii) $Y = (A + \overline{B})(A + C)$

iii) $Z = \overline{A}\,\overline{B}C + \overline{(A + \overline{B} + \overline{C})}$

(7 marks / markah)

(b) Refer to the following expression,

Merujuk pada persamaan yang berikut,

$$X = \overline{(\overline{A}B + C)} + CD$$

i) Draw the circuit using logic gates.
Lukiskan litar menggunakan get-get logik.

ii) Draw the circuits using minimum number of 2-inputs NAND gates only.
Lukiskan litar menggunakan get TAK DAN 2-masukan sahaja pada bilangan yang minimum.

(8 marks / *markah*)

(c) Figure Q2(c) shows three switches that are part of control circuitry in a photostat machine. The switches are at various points along the path of the copy paper as the paper passes through the machine. Each switch is normally open, and as the paper passes over a switch, the switch closes. It is impossible for SW 1 and SW 3 to be closed at the same time. An output, Y will be HIGH/Logic 1 whenever two or more switches are closed at the same time. Note: switch closed logic 0 and opened logic 1. SW 1 = A, SW 2 = B and SW 3 = C.

Rajah Q2(c) menunjukkan tiga suis iaitu sebahagian daripada litar kawalan di dalam mesin photostat. Suis-suis ini berada di titik-titik sepanjang laluan kertas salinan ketika bergerak melalui mesin. Setiap suis dalam keadaan buka, dan bila kertas melalui suis, suis akan tutup. Ianya tidak mungkin bagi SW 1 dan SW 3 tutup dalam masa yang sama. Keluaran, Y menjadi TINGGI/logik 1 bila mana dua atau lebih suis adalah tutup dalam masa yang sama. Nota: Suis tutup logik 0 dan buka logik 1. SW 1 = A, SW 2 = B dan SW 3 = C.

i) Produce a truth table.
Hasilkan jadual benar.

ii) Draw a simplified logic circuit.
Lukiskan litar logik yang teringkas.

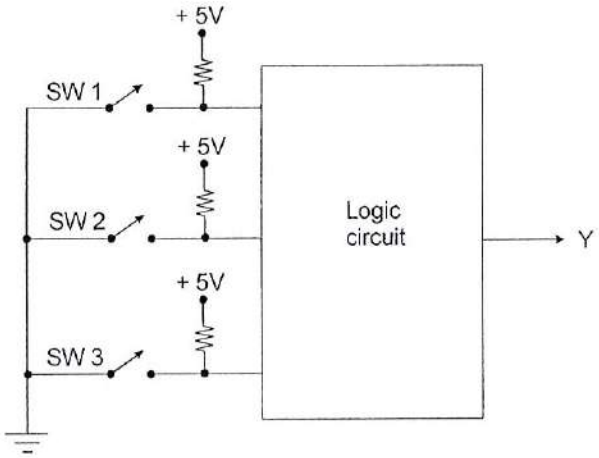


Figure Q2(c) / *Rajah Q2(c)*

(15 marks / *markah*)

Q3. (a) Draw the connection to 74283 IC as shown in Figure Q3(a) and add other gates (if necessary) for the arithmetic process $30_{10} - 17_{10}$ by using 2's complement method. Use 8-bit including the signed-bit. Datasheet of IC 74283 is given for reference.

Lakukan penyambungan ke atas IC 74283 seperti yang di tunjukkan pada Rajah Q3(a) dan tambah get-get lain (jika perlu) bagi proses arithmetik $30_{10} - 17_{10}$ dengan menggunakan kaedah pelengkap 2. Gunakan 8-bit termasuk bit tanda. Diberikan Lampiran data bagi IC 74283 untuk rujukan.

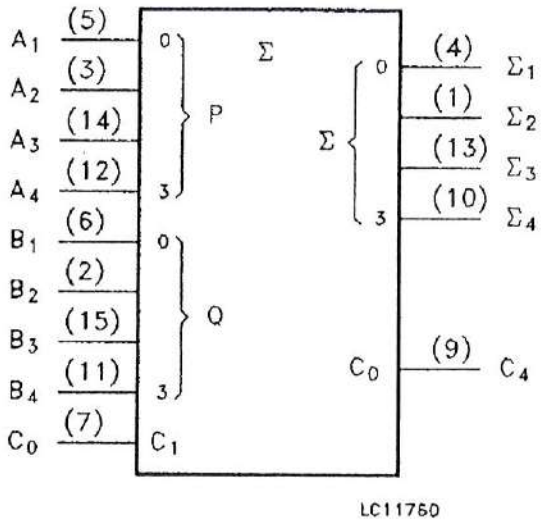


Figure Q3(a) / *Rajah Q3(a)*

(9 marks / *markah*)

(b) Produce a truth table for the circuit in Figure Q3(b).

Hasilkan jadual benar bagi litar di Rajah Q3(b).

(8 marks / *markah*)

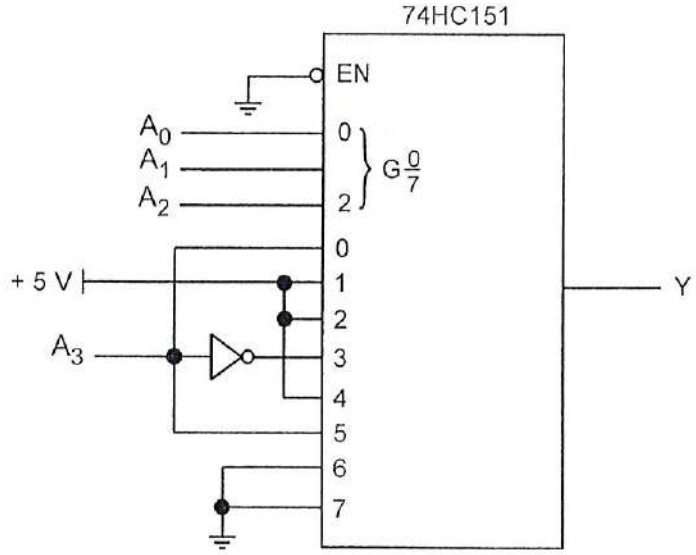


Figure Q3(b) / *Rajah Q3(b)*

Q4. (a) Refer to the circuit in Figure Q4(a)(i), draw the output waveform Q_1 and Q_2 in Figure Q4(a)(ii) in appendix. The output of flip-flop and latch are LOW at initial state.

Rujuk pada Rajah Q4(a)(i), lukiskan gelombang keluaran Q_1 dan Q_2 di dalam Rajah Q4(a)(ii) dalam lampiran. Keluaran bat[redacted]

Q5 (a) Determine the values of noise margin (HIGH & LOW) from the logic level shown in Figure Q5(a).

Tentukan nilai bagi jidar hingar (TINGGI & RENDAH) daripada aras logik dalam Rajah Q5(a).

(4 marks / *markah*)

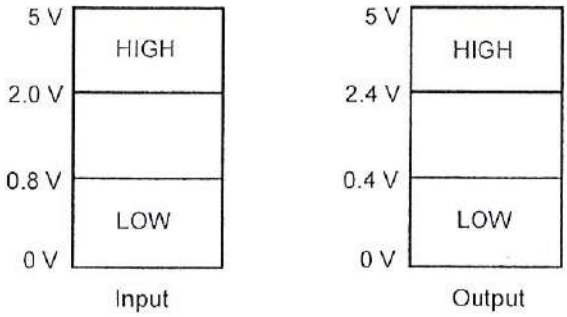


Figure Q5(a) / *Rajah Q5(a)*

(b) A data sheet for a standard TTL IC chip containing four NOR gates lists values of I_{CCH} = 6 mA, I_{CCL} = 16 mA and V_{CC} = 5V. Calculate the average power dissipated by each gate. Show your work.

Satu helaian data bagi serpih IC TTL standard yang mengandungi empat get NOR mempunyai senarai nilai-nilai berikut: = 6 mA, I_{CCL} = 16 mA and V_{CC} = 5V. Kira purata kelesapan kuasa bagi setiap get. Tunjukkan jalan kerja anda.

(6 marks / *markah*)

(c) Refer Figure Q5(c). Determine whether driving gates G_1, G_2 and G_3 is sourcing or sinking current. All gates are standard TTL.

Rujuk Rajah Q5(c). Tentukan samada get pemicu G_1, G_2 dan G_3 mengeluar atau menerima arus. Semua get adalah standard TTL.

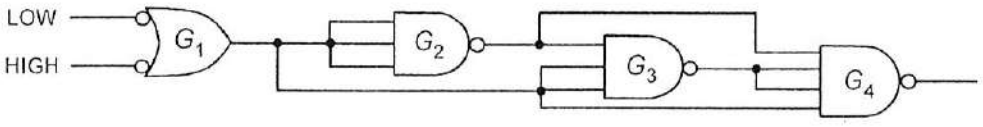


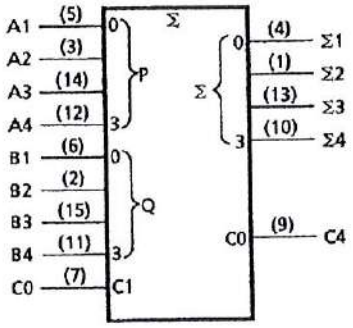
Figure Q5(c) / *Rajah Q5(c)*

(3 marks / *markah*)

DATA SHEET / *LAMPIRAN DATA*

TC74HC283AP, TC74HC283AF, TC74HC283AFN

IEC LOGIC SYMBOL



TRUTH TABLE (1bit)

INPUTS			OUTPUTS	
Bn	An	Cn−1	Σn	Cn
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

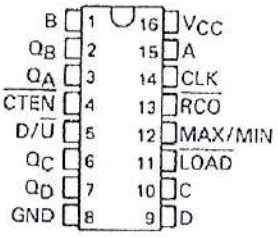
SN54190, SN54191, SN54LS190, SN54LS191, SN74190, SN74191, SN74LS190, SN74LS191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SDLS072 – DECEMBER 1972 – REVISED MARCH 1988

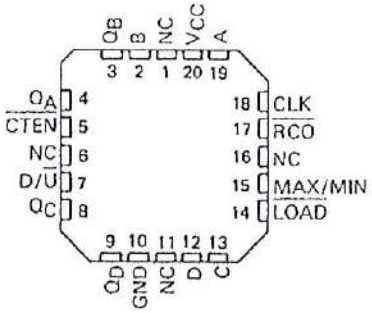
- Counts 8-4-2-1 BCD or Binary
- Single Down/Up Count Control Line
- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presettable with Load Control
- Parallel Outputs
- Cascadable for n-Bit Applications

TYPE	AVERAGE PROPAGATION DELAY	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'190,'191	20ns	25MHz	325mW
'LS190,'LS191	20ns	25MHz	100mW

SN54190, SN54191, SN54LS190, SN54LS191 . . . J PACKAGE
SN74190, SN74191 . . . N PACKAGE
SN74LS190, SN74LS191 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS190, SN54LS191 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

description

The '190, 'LS190, '191, and 'LS191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The '191 and 'LS191 are 4-bit binary counters and the '190 and 'LS190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter count up and when high, it counts down. A false clock may occur if the down/up input changes while the clock is low. A false ripple carry may occur if both the clock and enable are low and the down/up input is high during a load pulse.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made availeble to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

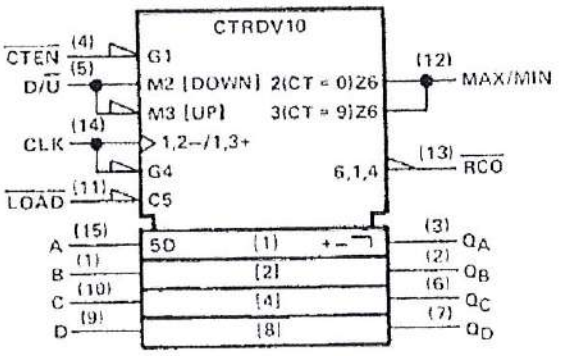
Series 54' and 54LS' are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74' and 74LS' are characterized for operation from 0°C to 70°C.

SN54190, SN54191, SN54LS190, SN54LS191, SN74190, SN74191, SN74LS190, SN74LS191 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

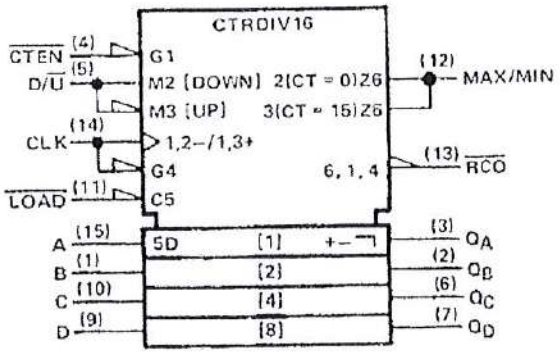
SDLS072 – DECEMBER 1972 – REVISED MARCH 1988

logic symbols†

'190, 'LS190



'191, 'LS191



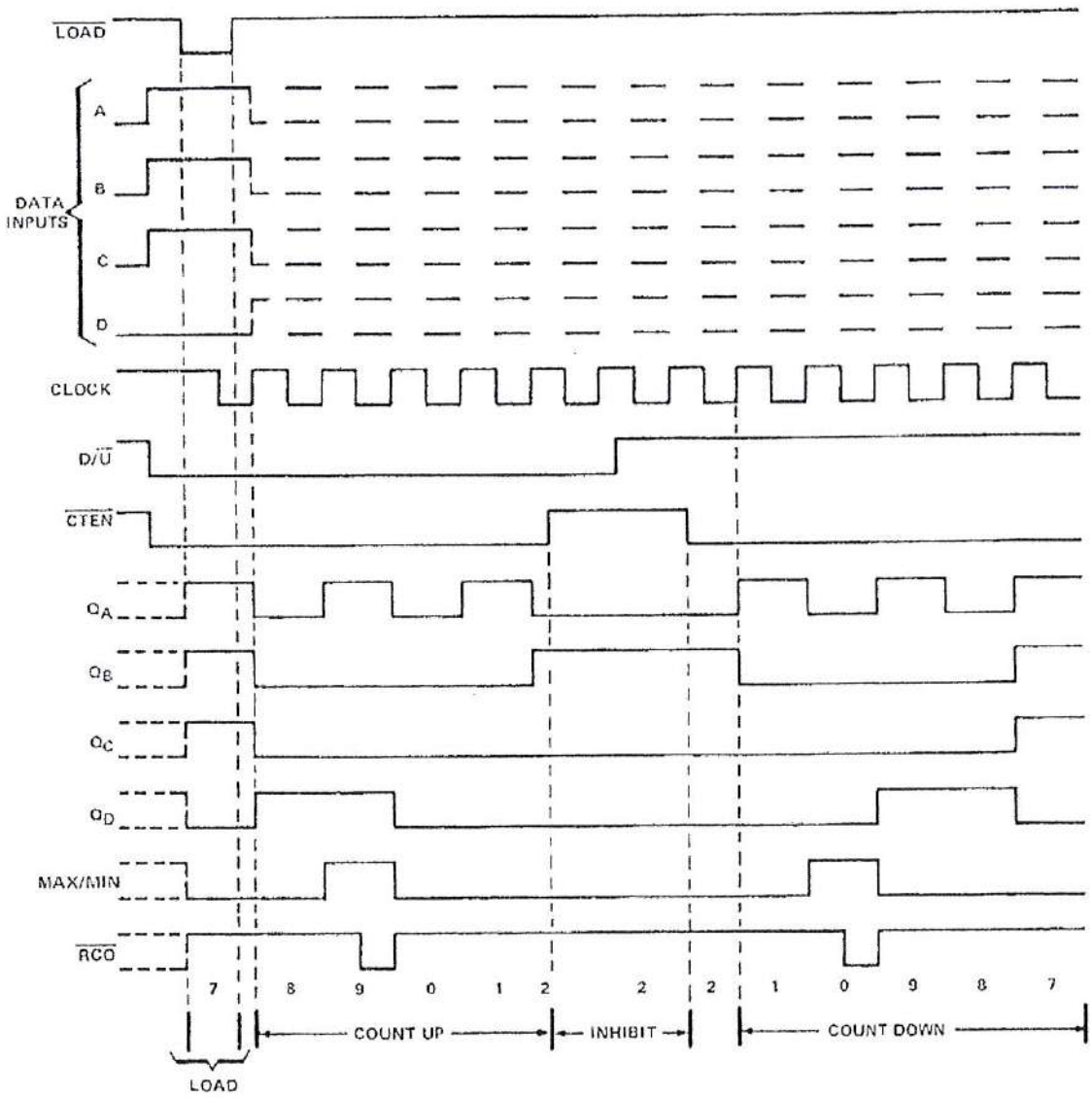
† These symbols are accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

'190, 'LS190 DECADE COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



Appendix / *Lampiran*

Name:_____

ID Number:_____

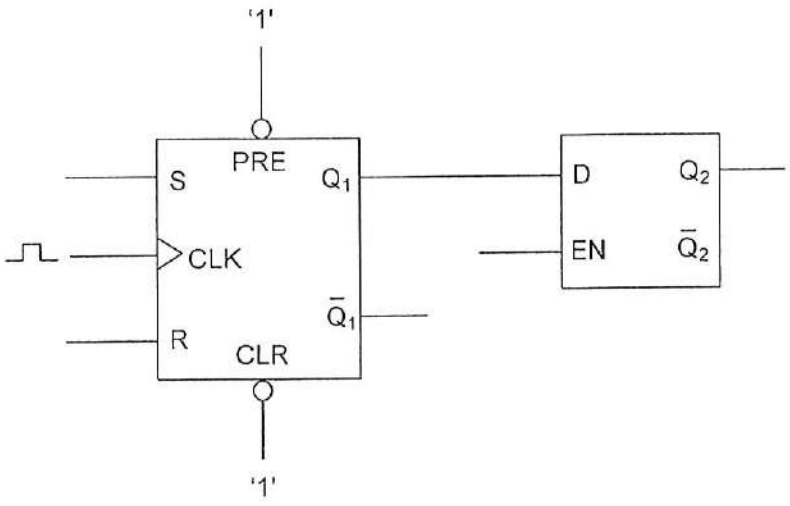


Figure Q4(a)(i) / *Rajah Q4(a)(i)*

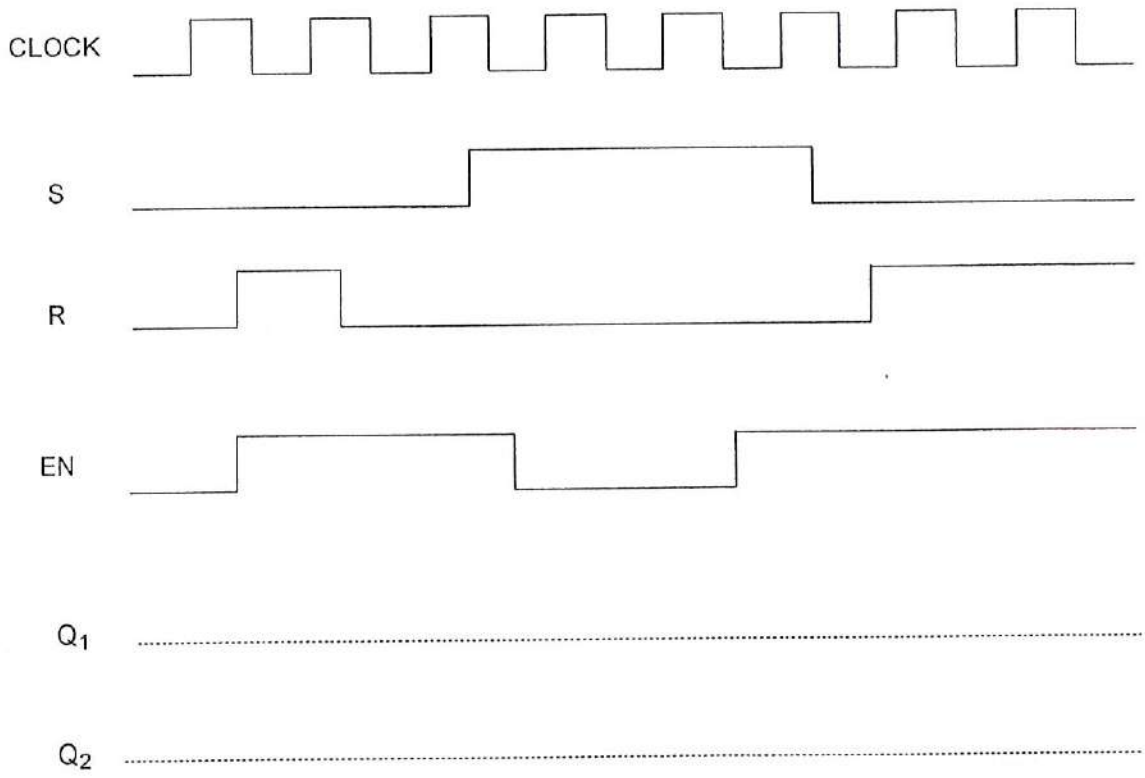


Figure Q4(a)(ii) / *Rajah Q4(a)(ii)*

Name:_____

ID Number:_____

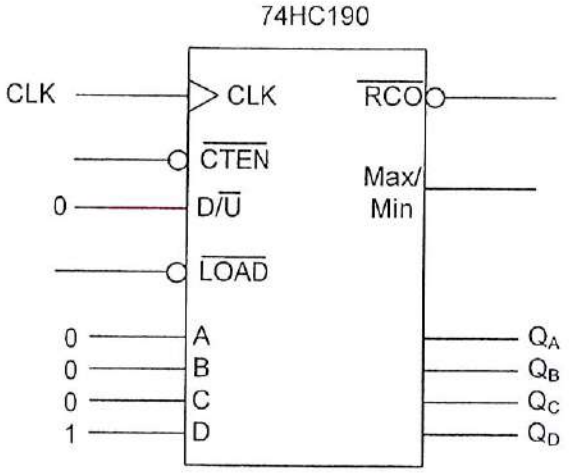


Figure Q4(c)(i) / *Rajah Q4(c)(i)*

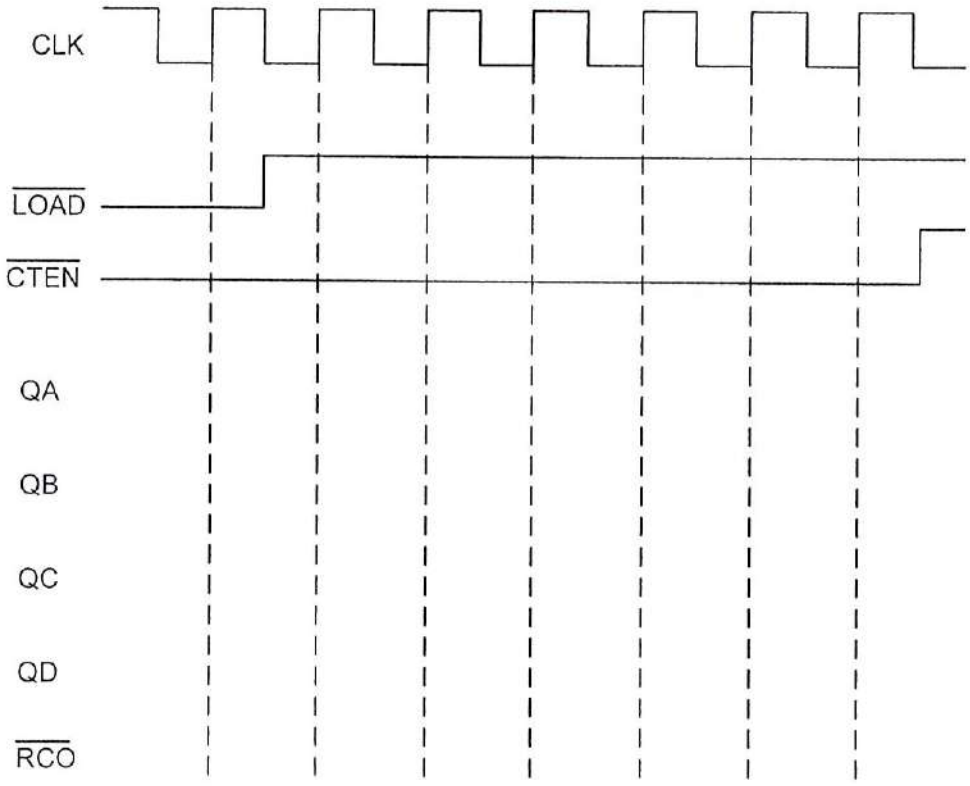


Figure Q4(c)(ii) / *Rajah Q4(c)(ii)*