UNIVERSITI TEKNOLOGI MALAYSIA

School of Professional and Continuing Education (SPACE)

FINAL EXAMINATION / *PEPERIKSAAN AKHIR*
SEMESTER I – SESSION 2021/ 2022 / *SEMESTER I – SESI 2021/2022*
PROGRAM KERJASAMA

COURSE CODE *KOD KURSUS*	: DDWE 2803 / DDKE 3023
COURSE NAME *NAMA KURSUS*	: MICROPROCESSOR *PEMPROSES MIKRO*
YEAR / PROGRAMME *TAHUN / PROGRAM*	: 2 DDWB/ DDWE/ DDWK/DTE
DURATION *TEMPOH*	: 3 HOURS (INCLUDING SUBMISSION HOUR) *3 JAM (TERMASUK MASA PENGHANTARAN)*
DATE *TARIKH*	: DECEMBER 2021 / JANUARY 2022 *DISEMBER 2021 / JANUARI 2022*

INSTRUCTION / *ARAHAN:*

1. Answer **ALL** questions and write your answers on the answer sheet.
   *Jawab **SEMUA** soalan dan tulis jawapan anda pada kertas jawapan.*

2. Write your name, matric no., identity card no., course code, course name, section no. and lecturer's name on the first page (in the upper left corner) and every page thereafter on the answer sheet.
   Tulis nama anda, no. matrik, no. kad pengenalan, kod kursus, nama kursus, no. seksyen dan nama pensyarah pada muka surat pertama(penjuru kiri atas)kertas jawapan dan pada setiap muka surat jawapan.

3. Each answer sheet must have a page number written at the bottom right corner.
   Setiap helai kertas jawapan mesti ditulis nombor muka surat pada bahagian bawah penjuru kanan.

4. Answers should be handwritten, neat and clear.
   Jawapan hendaklah ditulis tangan, kemas dan jelas menggunakan huruf cerai.

WARNING / *AMARAN*

Students caught copying / cheating during the examination will be liable for disciplinary actions and the faculty may recommend the student to be expelled from sitting for exam.
Pelajar yang ditangkap meniru / menipu semasa peperiksaan akan dikenakan tindakan disiplin dan pihak fakulti boleh mengesyorkan pelajar diusir dari menduduki peperiksaan.

This examination paper consists of **13** pages including the cover.
*Kertas soalan ini mengandungi **13** muka surat termasuk kulit hadapan.*

ONLINE EXAMINATION RULES AND REGULATIONS
PERATURAN PEPERIKSAAN SECARA DALAM TALIAN

1. Student must carefully listen and follow instructions provided by invigilator.

   Pelajar mesti mendengar dan mengikuti arahan yang diberikan oleh pengawas peperiksaan dengan teliti.

2. Student is allowed to start examination only after confirmation of invigilator if all needed conditions are implemented.

   Pelajar dibenarkan memulakan peperiksaan hanya setelah pengesahan pengawas peperiksaan sekiranya semua syarat yang diperlukan telah dilaksanakan.

3. During all examination session student has to ensure, that he is alone in the room.

   Semasa semua sesi peperiksaan pelajar harus memastikan bahawa dia bersendirian di dalam bilik.

4. During all examination session student is not allowed to use any other devices, applications except other sites permitted by course lecturer.

   Sepanjang sesi peperiksaan pelajar tidak dibenarkan menggunakan peranti dan aplikasi lain kecuali yang dibenarkan oleh pensyarah kursus.

5. After completing the exam student must inform invigilator via the set communication platform (eg. WhatsApp etc.) about completion of exam and after invigilator's confirmation leave examination session.

   Selepas peperiksaan selesai, pelajar mesti memaklumkan kepada pengawas peperiksaan melalui platform komunikasi yang ditetapkan (contoh: Whatsapp dan lain-lain) mengenai peperiksaan yang telah selesai dan meninggalkan sesi peperiksaan selepas mendapat pengesahan daripada pengawas peperiksaan.

6. Any technical issues in submitting answers online have to be informed to respective lecturer within the given 30 minutes. Request for re-examination or appeal will not be entertain if complains are not made by students to their lecturers within the given 30 minutes.

   Sebarang masalah teknikal dalam menghantar jawapan secara dalam talian perlu dimaklumkan kepada pensyarah masing-masing dalam masa 30 minit yang diberikan. Permintaan untuk pemeriksaan semula atau rayuan tidak akan dilayan sekiranya aduan tidak dibuat oleh pelajar kepada pensyarah mereka dalam masa 30 minit yang diberikan.

7. During online examination, the integrity and honesty of the student is also tested. At any circumstances student is not allowed to cheat during examination session. If any kind of cheating behaviour is observed, UTM have a right to follow related terms and provisions stated in the respective Academic Regulations and apply needed measures.

   Semasa peperiksaan dalam talian, integriti dan kejujuran pelajar juga diuji. Walau apa pun keadaan pelajar tidak dibenarkan menipu semasa sesi peperiksaan. Sekiranya terdapat sebarang salah laku, UTM berhak untuk mengikuti terma yang dinyatakan dalam Peraturan Akademik.

Excerpts from online final exam guidelines
Petikan daripada panduan peperiksaan akhir dalam talian
Universiti Teknologi Malaysia

Q1. For an 8051 system of 11.0592 MHz crystal, determine one machine cycle for the system.
Untuk suatu sistem 8051 dengan hablur 11.0592 MHz, tentukan satu kitaran mesin bagi sistem tersebut.

(2 marks/*markah*)

Q2. Determine how long does it take to execute each of the following instructions if one machine cycle of an 8051 system is 1 µs.
Tentukan berapa lama masa yang diambil untuk melaksanakan setiap arahan berikut jika satu kitaran mesin bagi satu sistem 8051 adalah 1 µs.

a) DIV AB
b) RL A

(4 marks/*markah*)

Q3. Show the status of the CY, AC and P flags after the execution of the following arithmetic instructions.
Tunjukkan status bendera CY, AC dan P setelah perlaksanaan arahan aritmetik berikut.

```
MOV  A,#93
ADD  A,#65
```

(5 marks/*markah*)

Q4. State the address of R3 after the execution of the following instruction.
Nyatakan alamat bagi R3 setelah arahan berikut dilaksanakan.

```
MOV  R3,#08H
MOV  PSW,R3
```

(2 marks/*markah*)

Q5. Convert **Program Q5** into machine codes (hex codes)**.**
*Tukarkan **Program Q5** kepada kod mesin (kod heks).*

```
        ORG   20H
ULANG:  MOV   DPTR,#0190H
        CLR   A
AGAIN:  MOVC  A,@A+DPTR
        JNZ   ULANG
        MOV   P2,A
        INC   DPTR
        SJMP  AGAIN
        END
```

Program Q5 (7 marks/*markah*)

Q6. What are the contents of the SP (Stack Pointer) upon RESET of the 8051?
Apakah kandungan SP (Penunjuk Tindanan) semasa 8051 di "RESET"?

(2 marks/*markah*)

Q7. Internal RAM of 8051 starting address 80H to FFH can only be accessed by using indirect addressing mode. Write an instruction(s) to store the value of 88H into the internal RAM at address location of AAH.
RAM dalaman bagi 8051 bermula pada alamat 80H hingga FFH hanya boleh dicapai dengan menggunakan ragam pengalamatan "indirect". Tulis arahan/arahan-arahan untuk mengisi nilai 88H ke dalam RAM dalaman pada lokasi alamat AAH.

(4 marks/*markah*)

Q8. Write a program to clear ACC and then add the value 3 to the ACC for ten times. Store the result in external memory at address location of 30H.
Tuliskan satu program untuk membersihkan ACC dan kemudian menambahkan ACC dengan nilai 3 sebanyak sepuluh kali. Simpan keputusannya pada ingatan luaran di lokasi alamat 30H.

(6 marks/*markah*)

Q9. For a machine cycle of 1 μs, calculate the time delay in the following subroutine.
Untuk kitaran mesin 1 μs, kirakan lengah masa dalam subrutin berikut.

```
HERE1:   MOV   R4,#64H   ;   1 cycle/kitar
HERE2:   MOV   R3,#255   ;   1 cycle/kitar
HERE3:   DJNZ  R3,HERE3  ;   2 cycle/kitar
         NOP             ;   1 cycle/kitar
         DJNZ  R4,HERE2  ;   2 cycle/kitar
         RET             ;   2 cycle/kitar
```

(5 marks/*markah*)

Q10. Write a program to add two(2) 6-digit Binary-Coded Decimal (BCD) numbers. First number is in memory locations 43H (MSB) 44H and 45H. Second number is in memory locations 40H (MSB), 41H and 42H. Place the BCD results in memory locations 43H (MSB) 44H and 45H.
Tuliskan program untuk menambah dua (2) nombor "Binary-Coded Decimal" (BCD) 6 digit. Nombor pertama terletak dalam lokasi alamat 43H (MSB), 44H dan 45H. Nombor kedua berada dalam lokasi ingatan 40H (MSB), 41H dan 42H. Letakkan keputusan hasil tambah nombor BCD berkenaan dalam lokasi ingatan 43H (MSB), 44H dan 45H.

(6 marks/*markah*)

Q11. The stack pointer contains F7H, accumulator A contains 0CCH and register B (F0H) contains 0DDH. What internal RAM locations are altered and what are the new values after executing the following instructions?
Note: PUSH direct ; (SP) ← (SP) + 1, ((SP)) ← (direct)
Penunjuk tindanan mengandungi nilai F7H, pengumpuk A mengandungi 0CCH dan daftar B (F0H) mengandungi nilai 0DDH. Apakah lokasi dalaman RAM yang berubah dan apakah nilai barunya setelah arahan-arahan berikut terlaksana?
Nota: PUSH direct ; (SP) ← (SP) + 1, ((SP)) ← (direct)

```
PUSH ACC
PUSH FOH
```

(4 marks/*markah*)

Q12. What is the content of memory location 80H after execution of **Program Q12**? Assume R0 contains the value of 80H. Show all workings.

*Apakah kandungan lokasi ingatan 80H setelah **Program Q12** terlaksana? Anggap R0 mengandungi nilai 80H. Tunjukkan jalan kerja.*

```
MOV   A,#58H
MOV   R5,#25H
ADD   A,R5
INC   DPTR
DA    A
MOV   @R0,A
```

Program Q12 (4 marks/*markah*)

Q13. Indicate which mode and which counter/timer is selected after the following instruction is executed.

Tentukan ragam dan pembilang/pemasa yang dipilih setelah arahan berikut terlaksana.

```
MOV   TMOD,#25H
```

(4 marks/*markah*)

Q14. If you are required to generate a square waveform on P1.0 with a frequency of 20 kHz having a duty cycle of 20%, what appropriate timer mode should you use? Why? Assume one machine cycle equal to 1 microsecond.

Sekiranya anda dikehendaki menjanakan gelombang segiempat berfrekuensi 20 kHz dengan kitar kerja 20% melalui P1.0, apakah ragam pemasa yang sesuai digunakan? Kenapa? Anggap satu kitaran mesin bersamaan 1 mikrosaat.

(6 marks/*markah*)

Q15. **Program Q15** is a delay subroutine in assembly language. Assuming a 12 MHz oscillator is used. How long does the timer take to overflow? Show your calculation to support your answer.
Program Q15 *adalah suatu subrutin lengah dalam bahasa himpunan. Anggap pengayun 12 MHz digunakan. Berapa lamakah masa diambil untuk pemasa tersebut mengalami limpahan? Tunjukkan pengiraan anda untuk menyokong jawapan yang diberikan.*

```
DELAY:   MOV   TMOD,#10H
AGAIN:   MOV   TH1,#0B1H
         MOV   TL1,#0E0H
         SETB  TR1
LOOP:    JNB   TF1,LOOP
         CLR   TR1
         CLR   TF1
         RET
```

Program Q15 (6 marks/*markah*)

Q16. What address in the interrupt vector table is assigned to INT0 and INT1? How about the pin numbers on Port-3 regarding both interrupts?
Apakah alamat dalam jadual sampukan vektor yang dikhususkan untuk INT0 dan INT1? Bagaimana pula nombor pin pada Liang-3 bagi kedua-dua sampukan berkenaan?

(4 marks/*markah*)

Q17. What register keeps track of interrupt priority in the 8051? Explain its role.
Apakah daftar yang memantau keutamaan sampukan dalam 8051? Terangkan tugasnya.

(3 marks/*markah*)

Q18. Write the instructions to enable the Timer 1 interrupt, Timer 0 interrupt, external interrupt 1 (INT1) and external interrupt 0 (INT0). External interrupt 1(INT1) has the highest priority.
Tuliskan arahan-arahan untuk membolehkan sampukan Pemasa 1, sampukan Pemasa 0, sampukan luaran 1 (INT1) dan sampukan luaran 0 (INT0). Sampukan luaran 1 (INT1) mempunyai keutamaan yang paling tinggi.

(4 marks/*markah*)

Q19. Discuss the sequence in which the interrupts are serviced for question Q18.
Bincangkan aturan jujukan di mana sampukan dilayan untuk soalan Q18.

(2 marks/markah)

Q20. A 4-bit DIP switch, U10, and a common-anode 7-segment display are connected to an 8051 microprocessor system as shown in Figure Q20. Write a program that continually reads a 4-bit code from the DIP switch, U10 and updates the segments to display the appropriate hexadecimal character. For example, if the code 0100B is read, the hexadecimal character "4" should appear. If an external interrupt-0 (INT0) occurs by detecting logic changes from high-to-low at pin INT0, the system should blink character "E" for 10 times.

Satu suis DIP 4-bit, U10, dan paparan 7-ruas anod sepunya disambungkan kepada satu sistem mikro pemproses 8051 seperti yang ditunjukkan pada Rajah Q20. Tuliskan satu program yang membaca secara berterusan kod 4-bit daripada suis DIP, U10 dan mengemaskini paparan pada ruas-ruas untuk memaparkan huruf heksadesimal yang tertentu. Sebagai contoh, jika kod 0100B dibaca, huruf heksadesimal "4" akan muncul. Apabila sampukan luaran-0 (INT0) berlaku dengan mengesan perubahan logik tinggi-ke-rendah pada pin INT0, sistem ini akan mengelipkan aksara "E" untuk 10 kali kelipan.

(20 marks/*markah*)

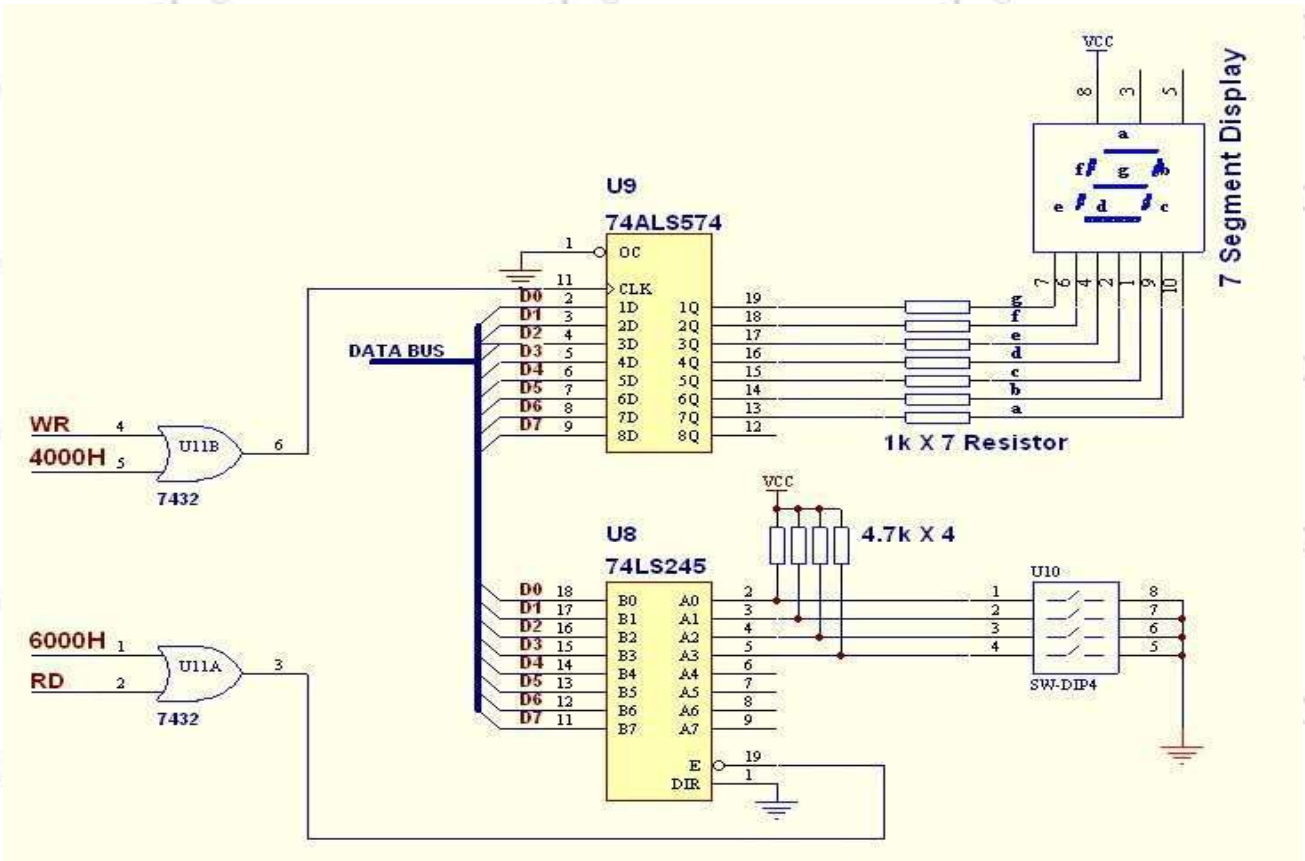
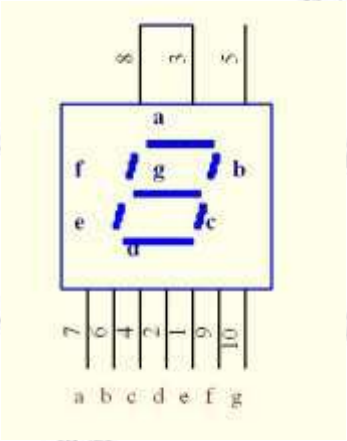


Figure Q20/ *Rajah Q20*

Seven Segment display lookup tables

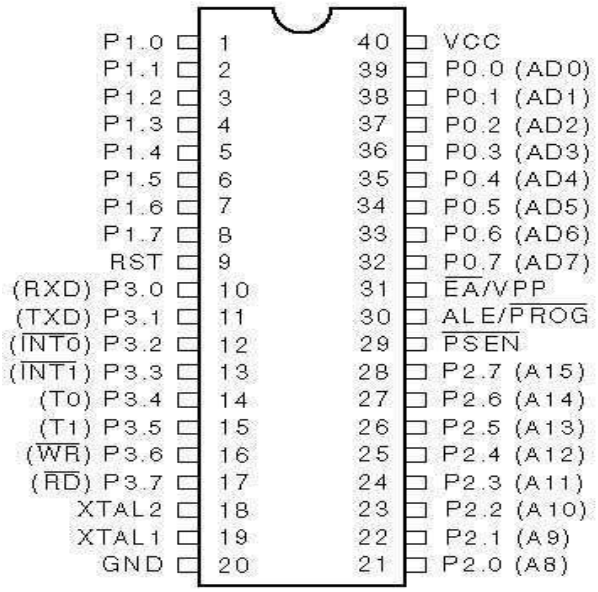


Display	Common Anode
0	81H
1	CFH
2	92H
3	86H
4	CCH
5	A4H
6	A0H
7	8FH
8	80H
9	8CH
A	88H
b	E0H
C	B1H
d	C2H
E	B0H
F	B8H
Blank	FFH

Instruction Code Summary

H / L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	JBC bit, rel	JB bit, rel	JNB bit, rel	JC rel	JNC rel	JZ rel	JNZ rel	SJMP rel	MOV DPTR, # data 16	ORL C, /bit	ANL C, /bit	PUSH dir	POP dir	MOVX A, @DPTR	MOVX @DPTR, A
1	AJMP (P0)	ACALL (P0)	AJMP (P1)	ACALL (P1)	AJMP (P2)	ACALL (P2)	AJMP (P3)	ACALL (P3)	AJMP (P4)	ACALL (P4)	AJMP (P5)	ACALL (P5)	AJMP (P6)	ACALL (P6)	AJMP (P7)	ACALL (P7)
2	LJMP addr16	LCALL addr16	RET	RETI	ORL dir, A	ANL dir, A	XRL dir, A	ORL C, bit	ANL C, bit	MOV bit, C	MOV C, bit	CPL bit	CLR bit	SETB bit	MOVX A, @R0	MOVX @R0, A
3	RR A	RRC A	RL A	RLC A	ORL dir, # data	ANL dir, # data	XRL dir, # data	JMP @A+DPTR	MOVC A, @A+PC	MOVC A, @A+DPTR	INC DPTR	CPL C	CLR C	SETB C	MOVX A, @R1	MOVX @R1, A
4	INC A	DEC A	ADD A, # data	ADDC A, # data	ORL A, # data	ANL A, # data	XRL A, # data	MOV A, # data	DIV AB	SUBB A, # data	MUL AB	CJNE A, # data, rel	SWAP A	DA A	CLR A	CPL A
5	INC dir	DEC dir	ADD A, dir	ADDC A, dir	ORL A, dir	ANL A, dir	XRL A, dir	MOV dir, # data	MOV dir, dir	SUBB A, dir		CJNE A, dir, rel	XCH A, dir	DJNZ dir, rel	MOV A, dir	MOV dir, A
6	INC @R0	DEC @R0	ADD A, @R0	ADDC A, @R0	ORL A, @R0	ANL A, @R0	XRL A, @R0	MOV @R0, # data	MOV dir, @R0	SUBB A, @R0	MOV @R0, dir	CJNE @R0, # data, rel	XCH A, @R0	XCHD A, @R0	MOV A, @R0	MOV @ R0, A
7	INC @R1	DEC @R1	ADD A, @R1	ADDC A, @R1	ORL A, @R1	ANL A, @R1	XRL A, @R1	MOV @R1, # data	MOV dir, @R1	SUBB A, @R1	MOV @R1, dir	CJNE @R1, # data, rel	XCH A, @R1	XCHD A, @R1	MOV A, @R1	MOV @ R1, A
8	INC R0	DEC R0	ADD A, R0	ADDC A, R0	ORL A, R0	ANL A, R0	XRL A, R0	MOV R0, # data	MOV dir, R0	SUBB A, R0	MOV R0, dir	CJNE R0, # data, rel	XCH A, R0	DJNZ R0, rel	MOV A, R0	MOV R0, A
9	INC R1	DEC R1	ADD A, R1	ADDC A, R1	ORL A, R1	ANL A, R1	XRL A, R1	MOV R1, # data	MOV dir, R1	SUBB A, R1	MOV R1, dir	CJNE R1, # data, rel	XCH A, R1	DJNZ R1, rel	MOV A, R1	MOV R1, A
A	INC R2	DEC R2	ADD A, R2	ADDC A, R2	ORL A, R2	ANL A, R2	XRL A, R2	MOV R2, # data	MOV dir, R2	SUBB A, R2	MOV R2, dir	CJNE R2, # data, rel	XCH A, R2	DJNZ R2, rel	MOV A, R2	MOV R2, A
B	INC R3	DEC R3	ADD A, R3	ADDC A, R3	ORL A, R3	ANL A, R3	XRL A, R3	MOV R3, # data	MOV dir, R3	SUBB A, R3	MOV R3, dir	CJNE R3, # data, rel	XCH A, R3	DJNZ R3, rel	MOV A, R3	MOV R3, A
C	INC R4	DEC R4	ADD A, R4	ADDC A, R4	ORL A, R4	ANL A, R4	XRL A, R4	MOV R4, # data	MOV dir, R4	SUBB A, R4	MOV R4, dir	CJNE R4, # data, rel	XCH A, R4	DJNZ R4, rel	MOV A, R4	MOV R4, A
D	INC R5	DEC R5	ADD A, R5	ADDC A, R5	ORL A, R5	ANL A, R5	XRL A, R5	MOV R5, # data	MOV dir, R5	SUBB A, R5	MOV R5, dir	CJNE R5, # data, rel	XCH A, R5	DJNZ R5, rel	MOV A, R5	MOV R5, A
E	INC R6	DEC R6	ADD A, R6	ADDC A, R6	ORL A, R6	ANL A, R6	XRL A, R6	MOV R6, # data	MOV dir, R6	SUBB A, R6	MOV R6, dir	CJNE R6, # data, rel	XCH A, R6	DJNZ R6, rel	MOV A, R6	MOV R6, A
F	INC R7	DEC R7	ADD A, R7	ADDC A, R7	ORL A, R7	ANL A, R7	XRL A, R7	MOV R7, # data	MOV dir, R7	SUBB A, R7	MOV R7, dir	CJNE R7, # data, rel	XCH A, R7	DJNZ R7, rel	MOV A, R7	MOV R7, A

2Byte	3Byte
2Cycle	4Cycle



Pin Configurations

The Program Status Word (PSW)

Bit	Symbol	Address	Description
PSW.7	CY	D7H	Carry flag
PSW.6	AC	D6H	Auxiliary carry flag
PSW.5	F0	D5H	Flag 0
PSW.4	RS1	D4H	Register bank select 1
PSW.3	RS0	D3H	Register bank select 0
PSW.2	OV	D2H	Overflow flag
PSW.1	--	D1H	Reserved
PSW.0	P	D0H	Parity Flag.

RS1	RS0	Bank	Address
0	0	0	00H – 07H
0	1	1	08H – 1FH
1	0	2	10H – 17H
1	1	3	18H – 1FH

Timer Control (TCON) register summary

Bit	SYMBOL	BIT ADDRESS	DESCRIPTION
TCON.7	TF1	8FH	Timer 1 overflow flag. Set by hardware upon overflow; cleared by software, or by hardware when processor vectors to interrupt service routine
TCON.6	TR1	8EH	Timer 1 run-control bit. Set/cleared by software to turn timer on/off
TCON.5	TF0	8DH	Timer 0 overflow bit. Do the same function as TF1 but for Timer 0
TCON.4	TR0	8CH	Timer 0 run-control bit. Do the same function as TR1 but for Timer 0
TCON.3	IE1	8BH	External interrupt 1 edge flag. Set by hardware when a falling edge is detected on INT1;cleared by software, or by hardware when CPU vectors to interrupt service routine
TCON.2	IT1	8AH	External interrupt 1 type flag. Set/cleared by software for falling edge/low-level activated external interrupt.
TCON.1	IE0	89H	External interrupt 0 edge flag. Do the same function as IE1 but for external interrupt-0.
TCON.0	IT0	88H	External interrupt 0 type flag. Do the same function as IT1 but for external interrupt-0.

Timer Mode (TMOD) register summary

Bit	Name	Timer	Description
7	GATE	1	When this bit is set the timer will only run when INT1(P3.3) is high(hardware control). When this bit is cleared the timer will run regardless of the state of INT1(software control.
6	C/T	1	Counter/timer select bit. 1 = counter operation 0 = timer operation
5	M1	1	Mode bit 1
4	M0	1	Mode bit 0
3	GATE	0	Timer 0 gate bit
2	C/T	0	Timer 0 counter/timer select bit
1	M1	0	Timer 0 M1 bit
0	M0	0	Timer 0 M0 bit

M1	M0	Mode	Description
0	0	0	13-bit timer mode (8048 mode)
0	1	1	16-bit timer mode
1	0	2	8-bit auto-reload mode
1	1	3	Split timer mode Timer 0: TL0 is an 8-bit timer controlled by timer 0 mode bits; TH0, the same except controlled by timer 1 mode bits Timer1: stopped

Table 6-1 Interrupt Enable (IE) register summary

Bit	Symbol	Bit Address	Description (1 = enable, 0 = disable)
IE.7	EA	AFH	Global enable/disable. EA = 1, each individual source is enabled/disabled by setting/clearing its enable bit. EA= 0, disable all interrupts.
IE.6	-	AEH	Undefined
IE.5	ET2	ADH	Enable Timer 2 interrupt(8052)
IE.4	ES	ACH	Enable serial port interrupt
IE.3	ET1	ABH	Enable Timer 1 interrupt
IE.2	EX1	AAH	Enable external 1 interrupt
IE.1	ET0	A9H	Enable Timer 0 interrupt
IE.0	EX0	A8H	Enable external 0 interrupt

Interrupt Priority (IP) Register

Bit	Symbol	Bit Address	Description (1 = Higher level, 0 = lower level)
IP.7	-	-	Undefined
IP.6	-	-	Undefined
IP.5	PT2	BDH	Priority for Timer 2 interrupt(8052)
IP.4	PS	BCH	Priority for serial port interrupt
IP.3	PT1	BBH	Priority for Timer 1 interrupt
IP.2	PX1	BAH	Priority for external 1 interrupt
IP.1	PT0	B9H	Priority for Timer 0 interrupt
IP.0	PX0	B8H	Priority for external 0 interrupt

Interrupt Vectors

Interrupt	Flag	Bit Address
System Reset	RST	0000H
External 0	IE0	0003H
Timer 0	TF0	000BH
External 1	IE1	0013H
Timer 1	TF1	001BH
SerialPort	RI or TI	0023H
Timer 2	TF2 or EXF2	002BH

Register values after system reset(power-up)

REGISTER(S)	CONTENTS
Program Counter	0000H
Accumulator	00H
B register	00H
PSW	00H
SP	07H
DPTR	0000H
Ports 0 – 3	FFH
IP	XXX00000B
Timer Register	00H
SCON	00H
SBUF	00H
PCON(HMOS)	0XXXXXXXB
PCON(CMOS)	0XXX0000B

END OF PAGE