UTM
UNIVERSITI TEKNOLOGI MALAYSIA

SekolahPendidikanProfesionaldan
PendidikanBerterusan
(UTMSPACE)

DDPB

FINAL EXAMINATION / *PEPERIKSAAN AKHIR*
SEMESTER 2 – SESSION 2015 / 2016
PROGRAM KERJASAMA

COURSE CODE *KOD KURSUS*	:	DDPE 1123
COURSE NAME *NAMA KURSUS*	:	DIGITAL ELECTRONIC / *ELEKTRONIK DIGITAL*
YEAR / PROGRAMME *TAHUN / PROGRAM*	:	1 DDPE/P/K/B
DURATION *TEMPOH*	:	2 HOURS 30 MINUTES / *2 JAM 30 MINIT*
DATE *TARIKH*	:	APRIL 2016

INSTRUCTION :

Q1. (a) Describe briefly the terms below :
Terangkan dengan ringkas istilah-istilah berikut:

i. Analog quantity / *kuantiti analog.*

ii. Decimal system / *sistem desimal.*

iii. Digital representations / *perwakilan digital.*

(3 marks/*markah*)

(b) Fill up Table Q1(b) with suitable entries.
Penuhkan Jadual Q1(b) dengan masukan yang sesuai.

Number of bits/ *Bilangan bit*	Unit of information/ *maklumat tentang unit*
(i)	nibble
8	(ii)
(iii)	word
32	(iv)

Table Q1(b) / *Jadual Q1(b)*

(4 marks/*markah*)

(c) (i) How many bytes are needed to represent 256_{10} in binary?
Berapakah bait yang diperlukan untuk mewakili 256_{10} dalam binari?

(ii) represent -27_{10} in 2's complement 8 bit signed number form.
wakilkan -27_{10} dalam bentuk pelengkap 2 nombor bertanda 8 bit.

(3 marks/*markah*)

(d) Perform the conversion:
Laksanakan penukaran:

i. **10011.101_2** to base-10 / *kepada kod asas-10*

ii. **127_{16}** to Gray code / *kepada kod Gray*

ii. **$010000110011_{\text{excess-3}}$** to octal / *kepada oktal*

(6 marks/*markah*)

(e) Perform an addition between 38 and 59 in BCD 8421 code and then attach an even parity bit to the left of MSB.
Laksanakan penambahan di antara 38 dan 59 dalam kod BCD 8421 dan kemudian sertakan bit pariti genap di kiri MSB.

(4 marks/*markah*)

Q2. (a) Simplify the following expression using deMorgan theorem and Boolean Algebra.
Ringkaskan persamaan-persamaan berikut menggunakan teorem deMorgan dan Aljabar Boolean.

i. $X = \overline{A\overline{B}\,(\overline{A+B})}$

ii. $Y = \overline{A+\overline{B}\,(A\overline{B}+\overline{A}B)(\overline{A+B})}$

iii. $Z = \overline{A\,B\,C}\,(\overline{A+B+C})$

(9 marks/*markah*)

(b) Refer to circuit in Figure Q2(b), simplify and implement the logic circuit by using 2 inputs NAND gates only.
Merujuk litar di dalam Rajah Q2(b), ringkaskan dan hasilkan litar logik menggunakan get TAK-DAN 2 masukan sahaja.

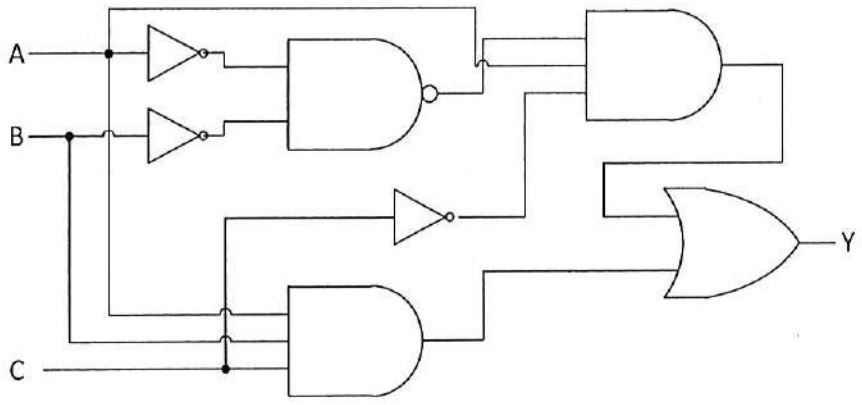


Figure Q2(b) / *Rajah Q2(b)*

(5 marks/*markah*)

(c) Figure Q2(c) shows a logic circuit diagram for a particular digital system that operated when the output Z is active-LOW. By employing alternative logic gates, draw the equivalent logic circuit representation to determine the possible input combinations to operate the digital system.

Rajah Q2(c) menunjukkan sebuah gambar rajah litar logik bagi satu sistem digital yang beroperasi apabila keluaran Z adalah aktif-RENDAH. Dengan mengunakan get-get logik alternatif, lukiskan perwakilan litar logik yang setara untuk menentukan kombinasi-kombinasi masukan yang berkemungkinan untuk membolehkan sistem digital tersebut beroperasi.

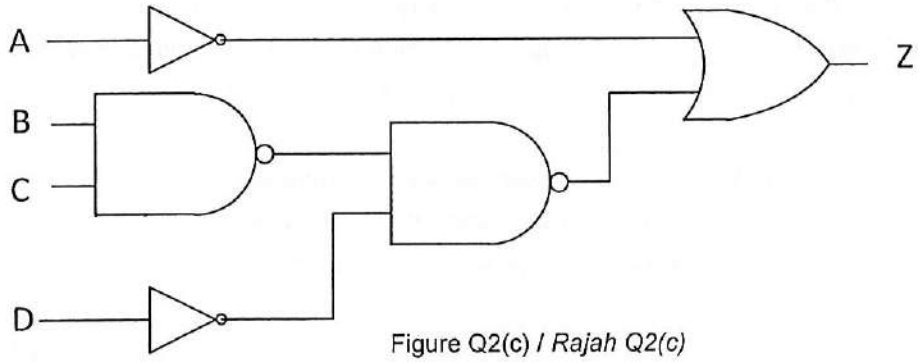


Figure Q2(c) / *Rajah Q2(c)*

(6 marks/*markah*)

Q3. A combinational circuit has three binary inputs B, S, I and three binary outputs, X, Y and Z. Each input represents an item that a person may order at a fast food place. The items are

B stands for burger	which cost = RM3
S stands for soda water	which cost = RM1
I stand for an ice cream	which cost = RM2

Each input can only be 1 or 0, which means that a customer can order only one (or none at all for B=0, S=0, I=0). The outputs represent a 3 bit encoding of the total cost of the order. For example, for B=1, S=1 and I=0 (which evaluates to RM 4) the output should be X=1, Y=0, Z=0.

i) Obtain the truth table for this combinational circuit

ii) Determine the minimum expression for X, Y and Z

iii) Construct logic circuits for the expression from (ii).

Sebuah litar gabungan mempunyai tiga masukan binary, B, S, I dan tiga keluaran binary, X, Y dan Z. Setiap masukan mewakili item yang mungkin pelanggan akan membuat pesanan di tempat makanan segera. Item-item tersebut adalah

B bermaksud burger	*yang berharga = RM3*
S bermaksud air soda	*yang berharga = RM1*
I bermaksud ais krim	*yang berharga = RM2*

Setiap masukan hanya boleh 1 atau 0, di mana bermaksud setiap pelanggan hanya boleh membuat pesanan sekali sahaja (atau tiada pesanan langsung , B=0, S=0, I=0). Keluaran mewakili pengekodan 3 bit bagi jumlah yang dipesan. Contohnya, bagi B=1, S=1 dan I=0 (di mana bernilai RM4) keluaran mestilah X=1, Y=0 dan Z=0.

i) Dapatkan jadual benar bagi litar gabungan tersebut.

ii) Tentukan penyataan yang minima bagi X, Y dan Z.

iii) Hasilkan litar-litar logik bagi penyataan dari (ii).

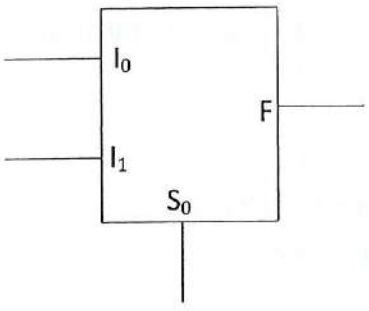
(20 marks/*markah*)

Q4. (a) How does a priority encoder differ from an ordinary encoder?
Bagaimanakah pengekod keutamaan berbeza dari pengekod biasa?

(3 marks/*markah*)

(b) Write the Booelan expression for the output F of the multiplexer in Figure Q4(b) in SOP form.
Tuliskan penyataan Boolean bagi keluaran F sebuah pemultipleks dalam Rajah Q4(b) dalam bentuk SOP.

Logic symbol / simbol logik



Truth table/ Jadual benar

S_0	F
0	I_0
1	I_1

Figure Q4(b) / *Rajah Q4(b)*

(5 marks/*markah*)

(c) Complete the timing diagram in Figure Q4(c)ii in the attachment by referring to Figure Q4(c)i. Assume the flip-flops are initially low.

Lengkapkan gambar rajah pemasaan di dalam Rajah Q4(c)ii di dalam lampiran dengan merujuk kepada Rajah Q4(c)i. Anggap keadaan awal bagi flip flop adalah rendah.

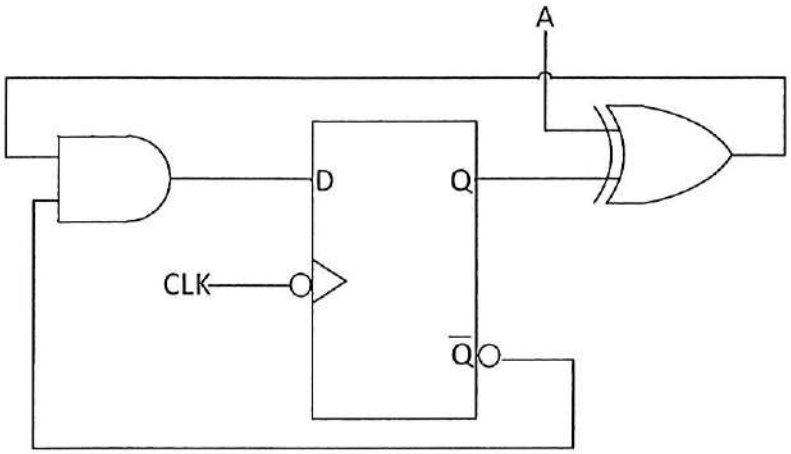


Figure Q4(c)(i) / *Rajah Q4(c)(i)*

(6 marks / *markah*)

(d) A 555 timer is configured to run as an astable multivibrator as shown in Figure Q4(d) determine;

Sebuah pemasa 555 dikonfigurasikan sebagai pemberbilang getar tidak stabil seperti yang ditunjukkan dalam Rajah Q4(d), tentukan;

(i) frequency / *frekuensi*

(ii) duty cycle / *kitar kerja*

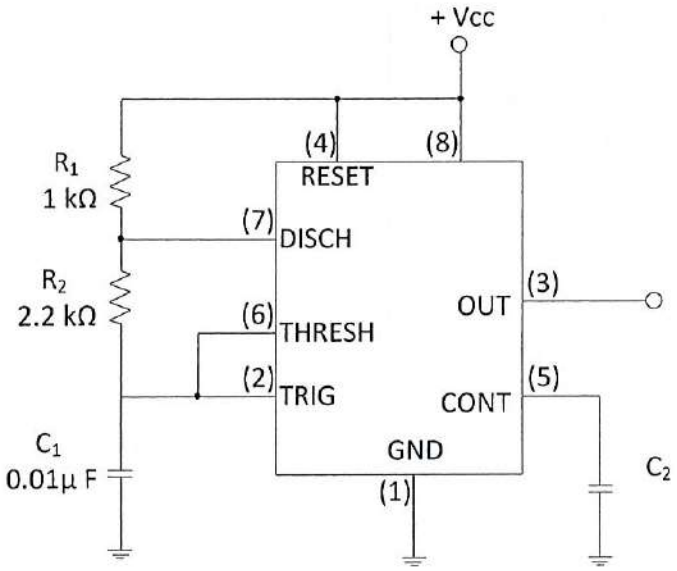


Figure Q4(d) / *Rajah Q4(d)*

(6 marks/*markah*)

Q5. (a) What is the suitable size of PAL (Programmable Array Logic) to implement the logic circuit as mentioned by the following Boolean expression and show the connection of the PAL.

Apakah saiz PAL yang sesuai untuk melaksanakan litar logik yang dinyatakan oleh persamaan Boolean berikut, serta tunjukkan sambungan PAL tersebut.

$$F_0 = \bar{A}BC + A\bar{B} + \bar{B}\bar{C}$$

$$F_1 = A + B\bar{C}$$

$$F_2 = A\bar{B} + \bar{A}B + A\bar{C}$$

(12 marks/*markah*)

(b) Referring to Figure Q5(b), determine the values of:

Merujuk kepada Rajah Q5(b), tentukan nilai-nilai berikut:

i. V_{IH}

ii. $V_{IH(min)}$ and $V_{IL(max)}$

iii. V_{OL}

iv. $V_{OH(min)}$ and $V_{OL(max)}$

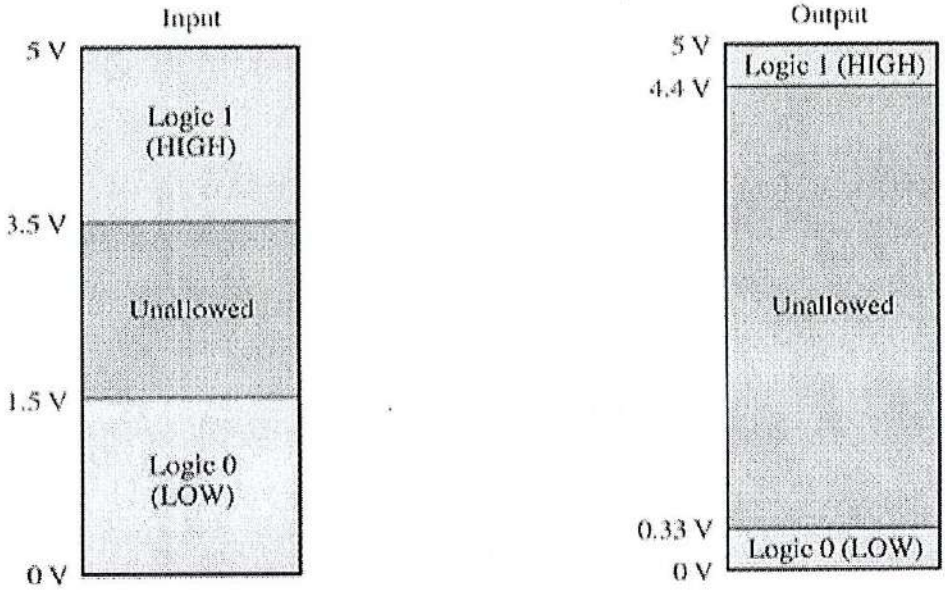


Figure Q5(b) / *Rajah Q5(b)*

(4 marks/*markah*)

(c) State the following term;

Nyatakan istilah berikut

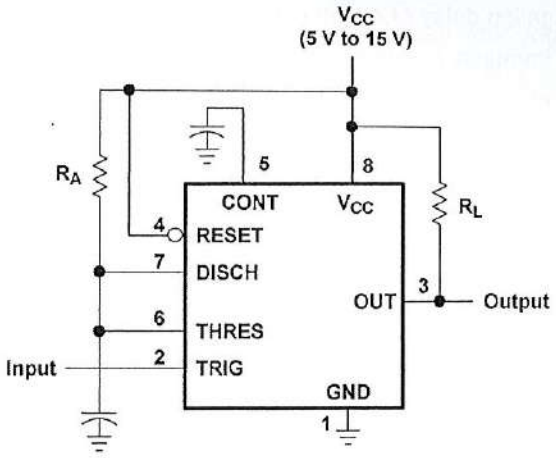
i) Propagation delay / *Lengah perambatan*

i) Noise immunity / *Imuniti hingar.*

ii) Fan-Out / *Rebak keluar*

(4 marks/*markah*)

Feature Description (continued)



Pin numbers shown are for the D, JG, P, PS, and PW packages.

Figure 9. Circuit for Monostable Operation

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high for at least 10 µs before the end of the timing interval. When the trigger is grounded, the comparator storage time can be as long as 10 µs, which limits the minimum monostable pulse width to 10 µs. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_w = 1.1R_AC$. Figure 11 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{CC}. The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to V_{CC}.

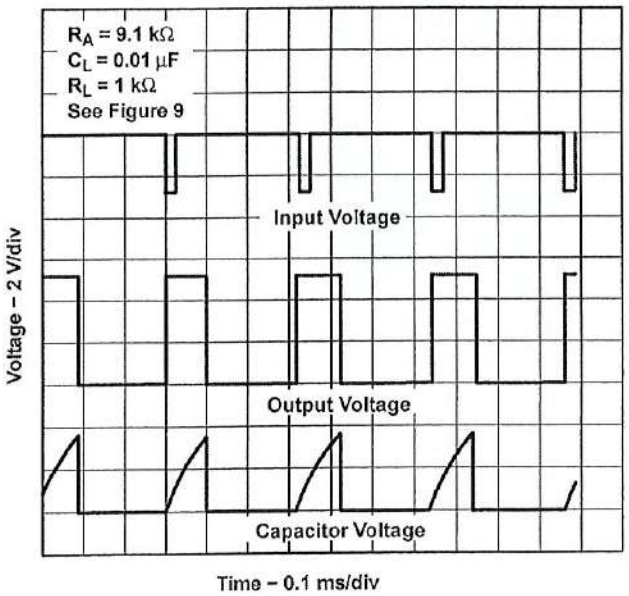


Figure 10. Typical Monostable Waveforms

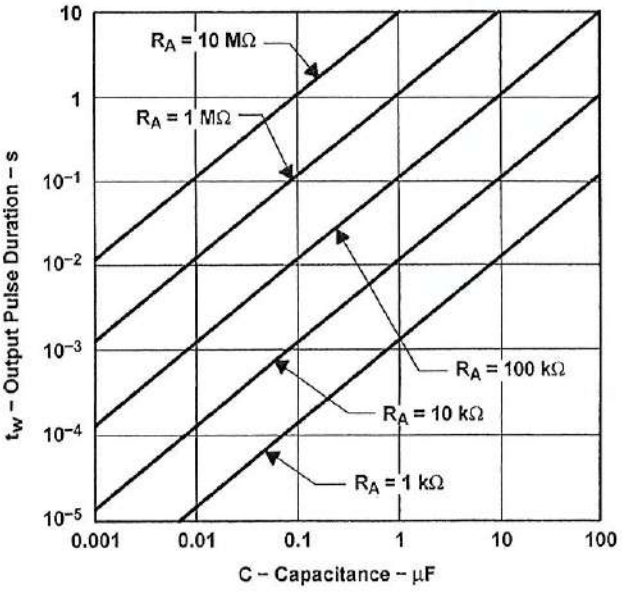


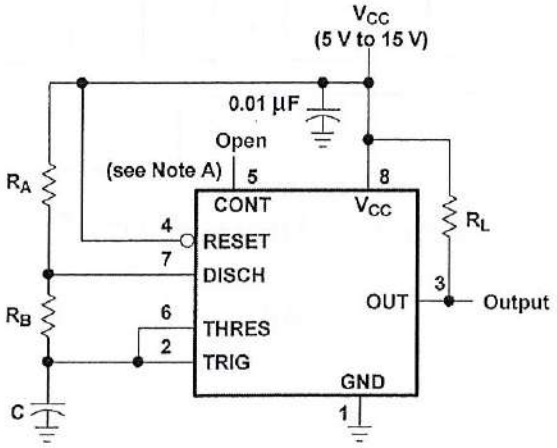
Figure 11. Output Pulse Duration vs Capacitance

Feature Description (continued)

8.3.2 A-stable Operation

As shown in Figure 12, adding a second resistor, R_B, to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multi-vibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level (≈ 0.67 × V_{CC}) and the trigger-voltage level (≈ 0.33 × V_{CC}). As in the mono-stable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 12. Circuit for Astable Operation

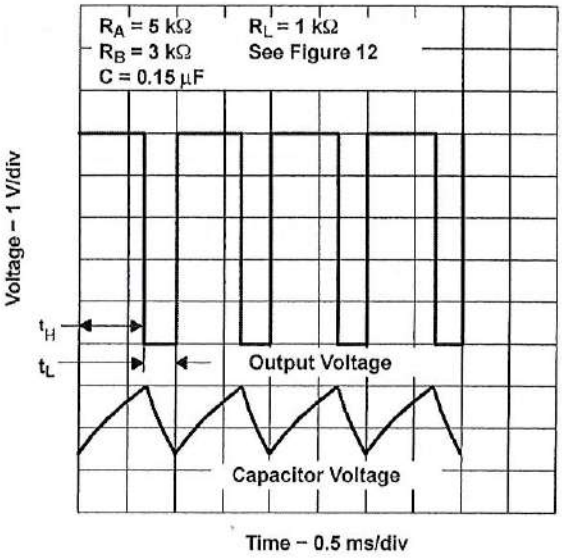


Figure 13. Typical Astable Waveforms

Figure 12 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L can be calculated as follows:

$$t_H = 0.693(R_A + R_B)C \quad (1)$$

$$t_L = 0.693(R_B)C \quad (2)$$

Other useful relationships are shown below:

$$\text{period} = t_H + t_L = 0.693(R_A + 2R_B)C \quad (3)$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)C} \quad (4)$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B} \quad (5)$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B} \quad (6)$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B} \quad (7)$$

Name:_____

ID Number:_____

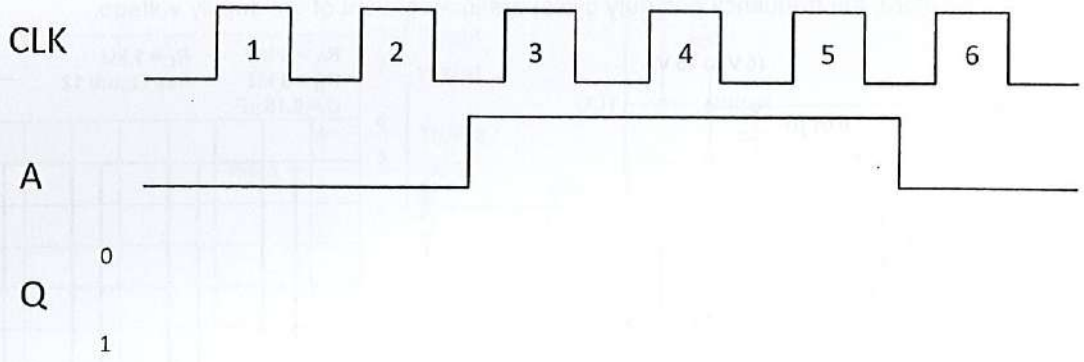


Figure Q4(c)ii / *Rajah Q4(c)ii*