KOLEJ YAYASAN PELAJARAN JOHOR
FINAL EXAMINATION

COURSE NAME	:	**ELECTRONIC CIRCUIT**
COURSE CODE	:	**DEE 1073**
EXAMINATION	:	**JUNE 2023**
DURATION	:	**2 HOURS 30 MINUTES**

INSTRUCTION TO CANDIDATES/
ARAHAN KEPADA CALON

1. This examination paper consists of **FOUR (4)** questions. /
*Kertas soalan ini mengandungi **EMPAT (4)** soalan.*

2. Candidates are not allowed to bring any material to examination room except with the permission from the invigilator. The formula was attached at the back question paper. /
Calon tidak dibenarkan untuk membawa sebarang bahan/nota ke bilik peperiksaan tanpa arahan/kebenaran daripada pengawas. Rumus dilampirkan di belakang kertas soalan peperiksaan.

3. Please check to make sure that this examination pack consists of: /
Pastikan kertas soalan peperiksaan ini mengandungi:
   i. Question Paper /
   Kertas Soalan
   ii. Answering Booklet /
   Buku Jawapan
   iii. Attachment 1 /
   Lampiran 1
   iv. Attachment 2 /
   Lampiran 2
   v. Attachment 3 /
   Lampiran 3

DO NOT TURN THIS PAGE UNTIL YOU ARE TOLD TO DO SO /
JANGAN BUKA KERTAS SOALAN INI SEHINGGA DIBERITAHU

This examination paper consists of **13** printed pages including front page
*Kertas soalan ini mengandungi **13** halaman bercetak termasuk muka hadapan*

This examination paper consists of **FOUR** (4) questions. Answer **ALL** the questions in the answer sheet.

*Kertas soalan ini mengandungi **EMPAT** (4) soalan. Jawab **SEMUA** soalan dalam buku jawapan.*

QUESTION 1/ *SOALAN 1*

The point of operation for transistor is known as quiescent point (Q-point). All three basic configuration for field effect transistor (FET) need Q-point to obtain the drain current and gate-to-source voltage.

a) Referring to **Figure 1(a)**, draw the transfer curve using shorthand method. The graph is given in the **Attachment 1**.

(10 marks/ *markah*)

b) Using the universal curve given in the **Attachment 2**, identify the values :

i) drain current, I_D

ii) gate-to-source voltage, V_{GS}

(5 marks/ *markah*)

c) Calculate :

i) drain-to-source voltage, V_{DS}

ii) source voltage, V_S

iii) drain voltage, V_D

iv) drain-to-gate voltage, V_{DG}

(9 marks/ *markah*)

b) If the value of R_S increased, what happen to Q-point?

(1 marks/ *markah*)

Titik operasi bagi transistor dikenali sebagai titik senyap (Q-point). Semua 3 konfigurasi asas bagi field effect transistor (FET) memerlukan Q-point untuk mendapatkan arus salir dan voltan get-sumber.

*a) Merujuk kepada **Rajah 1(a)**, lukiskan lengkuk pindah menggunakan kaedah shorthand. Graf diberi di **Lampiran 1**.*

b) Dengan menggunakan lengkuk universal yang diberi di **Lampiran 2**. *tetapkan jumlah :*

i) arus salir, I_D

ii) voltan get-sumber, V_{GS}

c) Kirakan :

i) voltan salir-sumber, V_{DS}

ii) voltan sumber, V_S

iii) voltan salir, V_D

iv) voltan salir-get, V_{DG}

d) Jika jumlah R_S *meningkat, apa akan terjadi terhadap Q-point?*

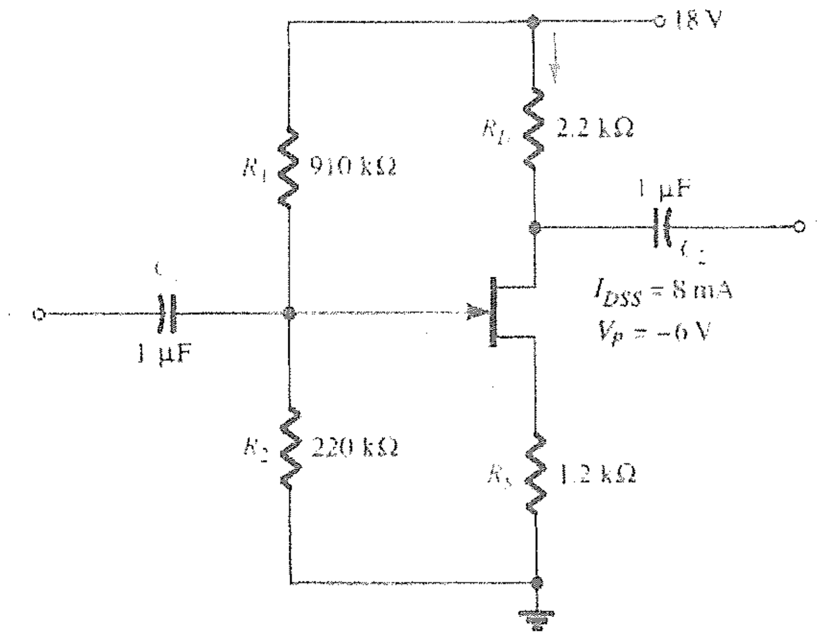


Figure 1(a) / *Rajah 1(a)*

QUESTION 2/ *SOALAN 2*

a) Calculate transconductance, g_m at V_{GS} = 0V for a JFET having device parameters I_{DSS} = 8mA and Vp = -5V.

(5 marks/ *markah*)

b) Given I_{DSS} = 6 mA, Vp = -6 V, g_{os} = 40 µS and V_{GSQ} = -2 V. Referring to **Figure 2(b)**, determine :

i) input impedance, Zi

ii) output impedance, Zo.

iii) voltage gain, Av

(**20 marks/ *markah***)

a) Kirakan kealiran pindah, g_m pada V_{GS} = 0V untuk JFET yang mempunyai parameter I_{DSS} = 8 mA dan Vp = -5 V.

*b) Diberi I_{DSS} = 6 mA, Vp = -6 V, g_{os} = 40 µS dan V_{GSQ} = -2 V. Merujuk kepada **Rajah 2(b)**, tentukan :*

i) input impedance, Zi

ii) output impedance, Zo

iii) voltage gain, Av.

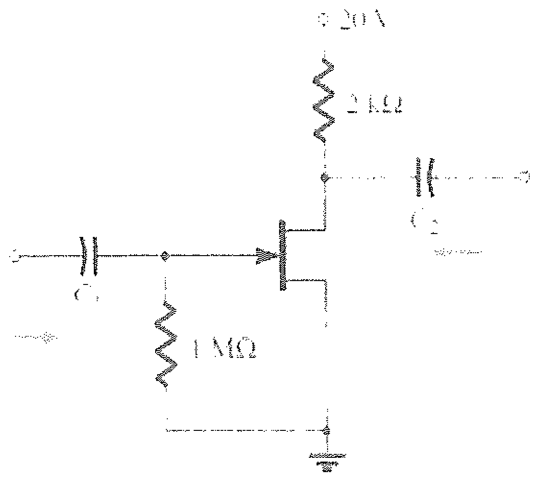


Figure 2(b) / *Rajah 2(b)*

QUESTION 3/ *SOALAN 3*

Differential operation involves the use of opposite-polarity inputs. Common-mode operation involves the use of the same-polarity inputs. Common-mode rejection ratio (CMRR) compares the gain for differential inputs to that for common inputs

a) Calculate the common-mode rejection ratio, CMRR (in dB) for the circuit measurements of V_{i1} = 200μV, V_{i2} = 140μV, Vo = 120mV, V_C = 1mV and Vd = 20μV.

(8 marks/ *markah*)

b) Calculate the output voltage for **Figure 3(b)** below. Given V_1 (rms) = 40mV and V_2 (rms) = 20mV.

(5 marks/ *markah*)

c) Referring to the operational amplifier circuit in **Figure 3(c)**, calculate the output voltages V_2 and V_3. Given V_1 = 0.2V.

(12 marks/ *markah*)

Operasi pembezaan melibatkan penggunaan masukan berlainan kekutuban. Operasi mod-biasa melibatkan penggunaan masukan kekutuban sama. Nisbah penolakan mod biasa (CMRR) membandingkan gandaan untuk masukan pembezaan terhadap masukan biasa.

a) Kirakan CMRR (dalam dB) bagi ukuran litar V_{i1} = 200 μV, V_{i2} = 140 μV, Vo = 120 mV, V_C = 1 mV, dan Vd = 20 μV.

b) Kirakan voltan keluaran bagi ***Rajah 3(b)*** *di bawah. Diberi V_1 (rms) = 40 mV dan V_2 (rms) = 20 mV.*

c) Merujuk kepada litar penguat kendalian dalam ***Rajah 3(c)****, kirakan voltan keluaran V_2 dan V_3. Diberi V_1 = 0.2 V.*

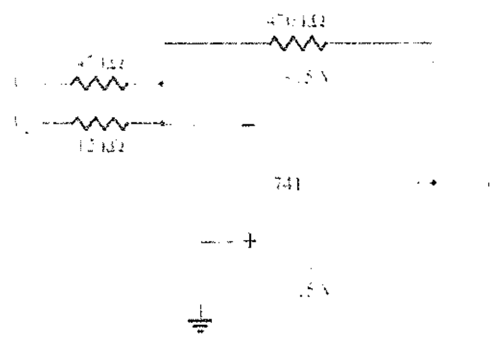


Figure 3(b) / *Rajah 3(b)*

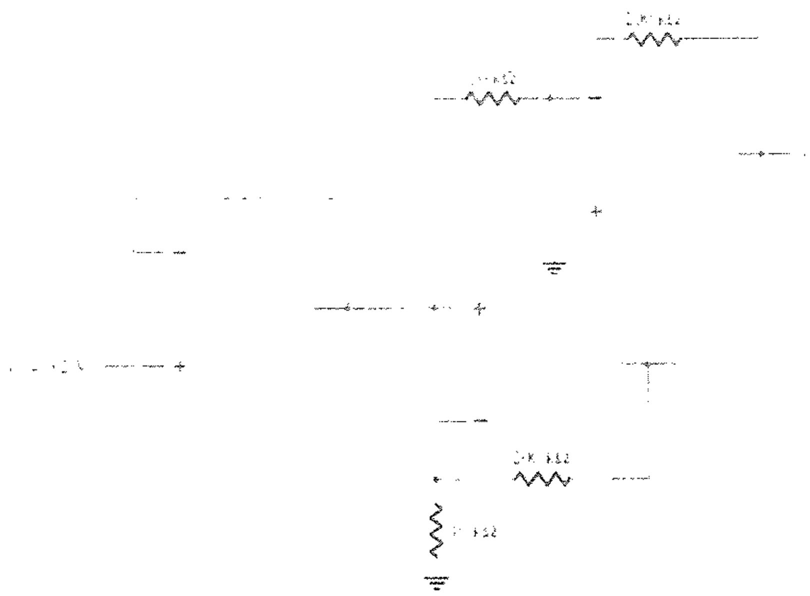


Figure 3(c) / *Rajah 3(c)*

QUESTION 4/ *SOALAN 4*

Power Amplifier can be categorized into several classes. Each class will be different in their operating cycle and efficiency. Based on Class B Power Amplifier circuit in **Figure 4**, calculate:

a) the peak input voltage, $V_{i(p)}$.
b) the peak voltage across the load, $V_{L(p)}$.
c) the peak load current, $I_{L(p)}$.
d) the direct current, I_{DC}.
e) the input power, $P_{in(dc)}$.
f) the output power, $P_{o(ac)}$.
g) the power dissipated by each output transistor, P_Q.
h) the circuit efficiency, %η.
i) the maximum input power, $P_{in(max)}$.
j) the maximum output power, $P_{o(max)}$.

(25 marks/ *markah*)

Penguat Kuasa boleh dikategorikan kepada beberapa kelas. Setiap kelas akan berbeza dari segi kitaran operasi dan kecekapan Berdasarkan litar Penguat Kuasa Kelas B dalam ***Rajah 4****, kirakan:*

a) voltan puncak merentasi masukan, $V_{i(p)}$
b) voltan puncak merentasi beban, $V_{L(p)}$
c) arus puncak pada beban, $I_{L(p)}$
d) arus terus, I_{DC}
e) kuasa masukan, $P_{in(dc)}$
f) kuasa keluaran, $P_{o(ac)}$
g) kuasa yang dilesapkan oleh setiap keluaran transistor, P_Q
h) kecekapan litar, %η.
i) kuasa masukan maksimum $P_{in(max)}$
j) kuasa keluaran maksimum $P_{o(max)}$.

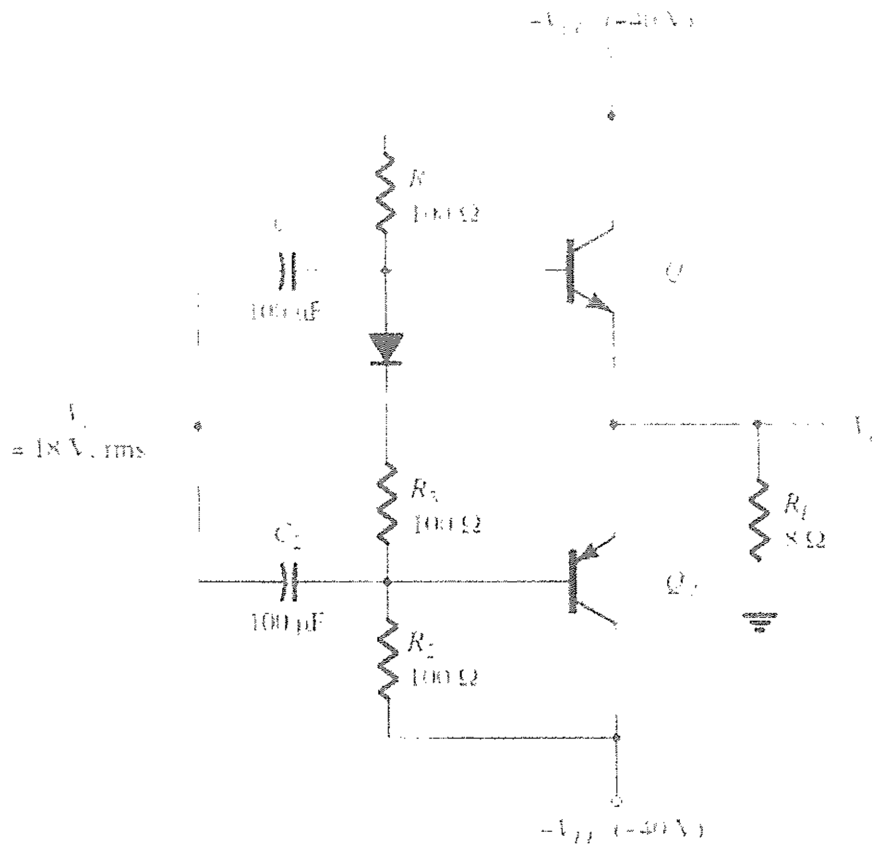


Figure 4 / *Rajah 4*

[100 MARKS/ *MARKAH*]

END OF QUESTION PAPER/ *KERTAS SOALAN TAMAT*

Attachment 1 / *Lampiran 1*

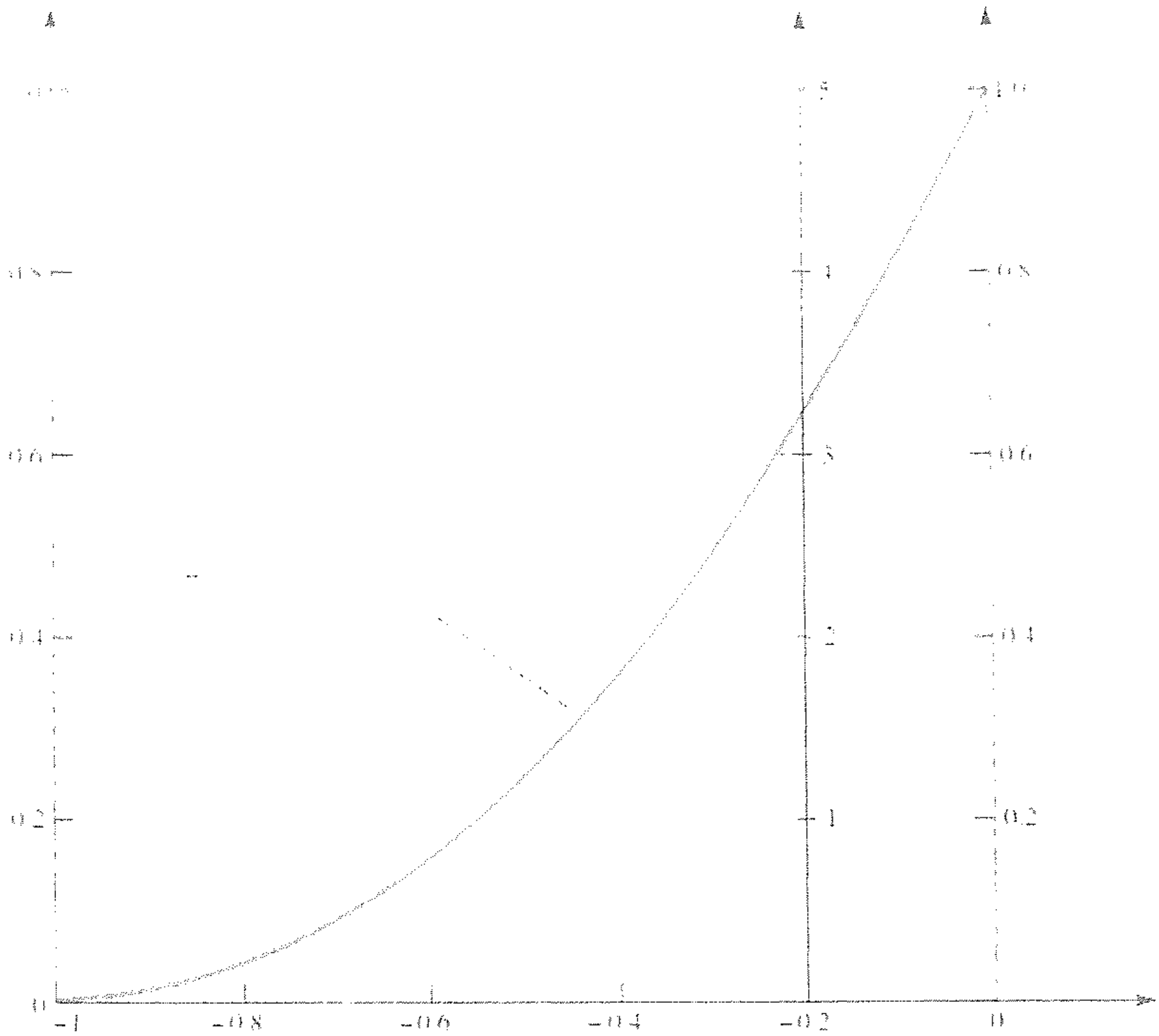
Name / *Nama* :..

Lecturer / *Pensyarah* :..

Attachment 2 / *Lampiran 2*

Name / *Nama* :..

Lecturer / *Pensyarah* :..



Attachment 3 / Lampiran 3

Formula / Rumus

JFET

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = I_{DSS}\big|_{V_{GS}=0\,V} \quad I_D = \frac{I_{DSS}}{2}\Big|_{V_{GS}=0.3V_P} \quad I_D = \frac{I_{DSS}}{4}\Big|_{V_{GS}=0.5V_P} \quad I_D = 0\,mA\big|_{V_{GS}=V_P}$$

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$I_G = 0\,A$$

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2}$$

MOSFET (enhancement)

$$I_D = k(V_{GS} - V_T)^2$$

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

JFETs/depletion-type MOSFETs

Fixed-bias configuration: $V_{GS} = -V_{GG} = V_G$

Self-bias configuration: $V_{GS} = -I_D R_S$

Voltage-divider biasing: $V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$

$V_{GS} = V_G - I_D R_S$

Enhancement-type MOSFETs

Feedback biasing: $V_{DS} = V_{GS}$

$V_{GS} = V_{DD} - I_D R_D$

Voltage-divider biasing: $V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$

$V_{GS} = V_G - I_D R_S$

$$g_m = y_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$g_{m0} = \frac{2 I_{DSS}}{|V_P|}$$

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$g_m = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

$$r_d = \frac{1}{y_{os}} = \frac{\Delta V_{DS}}{\Delta I_D}\bigg|_{V_{GS}=\text{constant}}$$

$$CMRR = [illegible]$$

Inverting amplifier

$$[illegible] = -[illegible]$$

Noninverting amplifier

$$[illegible] = [illegible]$$

[illegible]

$$[illegible] = [illegible]$$

Summing amplifier

$$V_o = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right)$$

Integrator amplifier

$$v_o(t) = -\frac{1}{R_1 C} \int v_1(t)\, dt$$

$$\text{Slew rate (SR)} = \frac{\Delta V_o}{\Delta t} \quad V/\mu s$$

Constant-gain multiplier

$$A = -\frac{R_f}{R_1}$$

Noninverting constant-gain multiplier

$$A = 1 + \frac{R_f}{R_1}$$

Voltage-summing amplifier

$$V_o = -\left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right]$$

Voltage buffer

$$V_o = V_1$$

Low-pass active filter cutoff frequency

$$f_{OH} = \frac{1}{2\pi R_1 C_1}$$

High-pass active filter cutoff frequency

$$f_{OL} = \frac{1}{2\pi R_1 C_1}$$

[illegible]

[illegible]

$= I_{C}^2 [illegible]$

$= [illegible]$

$[illegible] = \frac{[illegible]}{[illegible]}$

$= \frac{[illegible]}{2R}$

$= \frac{V_{CC}^2}{2R_L}$

$P_o(ac) = \frac{V_C(p\text{-}p)\, I_C(p\text{-}p)}{8}$

$= \frac{I_C^2(p\text{-}p)}{8} R_L$

$= \frac{V_C^2(p\text{-}p)}{8R_L}$

$\%\eta = \frac{P_o(ac)}{P_i(dc)} \times 100\%$

Transformer action

$$\frac{V_2}{V_1} = \frac{N_2}{N_1}$$

$$\frac{I_2}{I_1} = \frac{N_1}{N_2}$$

$$I_{dc} = \frac{2}{\pi} I(p)$$

$$P_i(dc) = V_{CC}\left(\frac{2}{\pi} I(p)\right)$$

$$P_o(ac) = \frac{V_L^2(rms)}{R_L}$$

$$\text{maximum } P_o(ac) = \frac{V_{CC}^2}{2R_L}$$

$$\text{maximum } P_i(dc) = V_{CC}(\text{maximum } I_{dc}) = V_{CC}\left(\frac{2V_{CC}}{\pi R_L}\right) = \frac{2V_{CC}^2}{\pi R_L}$$

$$\text{maximum } P_{2Q} = \frac{2V_{CC}^2}{\pi^2 R_L}$$

Harmonic distortion

$$n\text{th harmonic distortion} = \% D_n = \frac{|A_n|}{|A_1|} \times 100\%$$

Heat sink

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$