UNIVERSITI TEKNOLOGI MALAYSIA

Sekolah Pendidikan Profesional dan Pendidikan Berterusan (SPACE)

FINAL EXAMINATION / *PEPERIKSAAN AKHIR*
SEMESTER 2 – SESSION 2021 / 2022 / *SEMESTER 2 – SESI 2021 / 2022*
PROGRAM KERJASAMA

COURSE CODE *KOD KURSUS*	:	DDWE 2803
COURSE NAME *NAMA KURSUS*	:	MICROPROCESSOR *MIKROPEMPROSES*
YEAR / PROGRAMME *TAHUN / PROGRAM*	:	3 DDWB
DURATION *TEMPOH*	:	3 HOURS (INCLUDING SUBMISSION HOUR) *3 JAM (TERMASUK MASA PENGHANTARAN)*
DATE *TARIKH*	:	JUNE/JULY 2022 *JUN/JULAI 2022*

INSTRUCTION :
ARAHAN

1. Answer **ALL** questions and write your answers on the answer sheet.
   *Jawab **SEMUA** soalan dan tulis jawapan anda pada kertas jawapan.*

2. Write your name, matric no., identity card no., course code, course name, section no. and lecturer's name on the first page (in the upper left corner) and every page thereafter on the answer sheet.
   Tulis nama anda, no. matrik, no. kad pengenalan, kod kursus, nama kursus, no. seksyen dan nama pensyarah pada muka surat pertama (penjuru kiri atas) kertas jawapan dan pada setiap muka surat jawapan.

3. Each answer sheet must have a page number written at the bottom right corner.
   Setiap helai kertas jawapan mesti ditulis nombor muka surat pada bahagian bawah penjuru kanan.

4. Answers should be handwritten, neat and clear.
   Jawapan hendaklah ditulis tangan, kemas dan jelas menggunakan huruf cerai.

WARNING / *AMARAN*

Students caught copying / cheating during the examination will be liable for disciplinary actions and the faculty may recommend the student to be expelled from sitting for exam.
Pelajar yang ditangkap meniru / menipu semasa peperiksaan akan dikenakan tindakan disiplin dan pihak fakulti boleh mengesyorkan pelajar diusir dari menduduki peperiksaan.

This examination paper consists of 13 pages including the cover
Kertas soalan ini mengandungi 13 muka surat termasuk kulit hadapan

ONLINE EXAMINATION RULES AND REGULATIONS

PERATURAN PEPERIKSAAN SECARA DALAM TALIAN

1. Student must carefully listen and follow instructions provided by invigilator.
   Pelajar mesti mendengar dan mengikuti arahan yang diberikan oleh pengawas peperiksaan dengan teliti.

2. Student is allowed to start examination only after confirmation of invigilator if all needed conditions are implemented.
   Pelajar dibenarkan memulakan peperiksaan hanya setelah pengesahan pengawas peperiksaan sekiranya semua syarat yang diperlukan telah dilaksanakan.

3. During all examination session student has to ensure, that he is alone in the room.
   Semasa semua sesi peperiksaan pelajar harus memastikan bahawa dia bersendirian di dalam bilik.

4. During all examination session student is not allowed to use any other devices, applications except other sites permitted by course lecturer.
   Sepanjang sesi peperiksaan pelajar tidak dibenarkan menggunakan peranti dan aplikasi lain kecuali yang dibenarkan oleh pensyarah kursus.

5. After completing the exam student must inform invigilator via the set communication platform (eg. WhatsApp etc.) about completion of exam and after invigilator's confirmation leave examination session.
   Selepas peperiksaan selesai, pelajar mesti memaklumkan kepada pengawas peperiksaan melalui platform komunikasi yang ditetapkan (contoh: Whatsapp dan lain-lain) mengenai peperiksaan yang telah selesai dan meninggalkan sesi peperiksaan selepas mendapat pengesahan daripada pengawas peperiksaan.

6. Any technical issues in submitting answers online have to be informed to respective lecturer within the given 30 minutes. Request for re-examination or appeal will not be entertain if complains are not made by students to their lecturers within the given 30 minutes.
   Sebarang masalah teknikal dalam menghantar jawapan secara dalam talian perlu dimaklumkan kepada pensyarah masing-masing dalam masa 30 minit yang diberikan. Permintaan untuk pemeriksaan semula atau rayuan tidak akan dilayan sekiranya aduan tidak dibuat oleh pelajar kepada pensyarah mereka dalam masa 30 minit yang diberikan.

7. During online examination, the integrity and honesty of the student is also tested. At any circumstances student is not allowed to cheat during examination session. If any kind of cheating behaviour is observed, UTM have a right to follow related terms and provisions stated in the respective Academic Regulations and apply needed measures.
   Semasa peperiksaan dalam talian, integriti dan kejujuran pelajar juga diuji. Walau apa pun keadaan pelajar tidak dibenarkan menipu semasa sesi peperiksaan. Sekiranya terdapat sebarang salah laku, UTM berhak untuk mengikuti terma yang dinyatakan dalam Peraturan Akademik.

Excerpts from online final exam guidelines

Petikan daripada panduan peperiksaan akhir dalam talian

Universiti Teknologi Malaysia

Q1. Every 8051 family member starts its program at address _____ when it is powered up.
Setiap ahli keluarga 8051 memulakan aturcara pada alamat _____ apabila ianya dihidupkan.

(2 marks/*markah*)

Q2. In the 8051, the program counter is _____bits wide.
Dalam 8051, pembilang aturcara adalah bersaiz _____ bit.

(2 marks/*markah*)

Q3. Which register of the CPU holds the address of the instruction to be fetched?
Daftar manakah dalam CPU yang memegang alamat arahan yang akan dipungut?

(2 marks/*markah*)

Q4. Which section of the CPU is responsible for performing addition?
Bahagian manakah dalam CPU yang bertanggungjawab melaksanakan penambahan?

(2 marks/*markah*)

Q5. How many bytes of data can be addressed by a computer system with an 16-bit address bus and an 8-bit data bus?
Berapa bait data yang boleh dialamatkan oleh suatu sistem komputer yang mengandungi bas alamat 16 bit dan bas data 8 bit?

(2 marks/*markah*)

Q6. State the address of R5 after the execution of the following instruction.
Nyatakan alamat bagi R5 setelah arahan berikut dilaksanakan.

SETB PSW.4

(2 marks/*markah*)

Q7. On power-up, the 8051 uses RAM location _____ as the first location of the stack.
Semasa dihidupkan, 8051 menggunakan lokasi RAM _____ sebagai lokasi permulaan tindanan.

(2 marks/*markah*)

Q8. The 8051 CPU is reset if the RST pin is held HIGH for a minimum of 2 machine cycles. If an 8051 is operating from an 11.0592 MHz crystal, what is the minimum length of time for RST to be HIGH to achieve a system reset?
CPU 8051 adalah diresetkan jika pin RST dipegang pada logik TINGGI paling minimum selama 2 kitaran mesin. Jika 8051 beroperasi menggunakan hablur 11.0592 Mhz, apakah masa minimum untuk RST berada pada logik TINGGI supaya reset sistem tercapai?

(4 marks / *markah*)

Q9. Show the status of the CY, AC, and P flags after the execution of the following arithmetic instructions.
Tunjukkan status bendera CY, AC dan P setelah perlaksanaan arahan aritmatik berikut.

MOV A,#9CH
ADD A,#64H

(4 marks/*markah*)

Q10. Name the 8051 control bus signals used to select external EPROMs and external RAMs.
Namakan isyarat-isyarat bas kawalan 8051 yang digunakan untuk memilih EPROM luaran dan RAM luaran.

(3 marks/*markah*)

Q11. The stack pointer contains 7H, accumulator A contains 55H and register B (F0H) contains 4AH. What internal RAM locations are altered and what are the new values after executing the following instructions?
Penunjuk tindanan mengandungi nilai 7H, pengumpuk A mengandungi 55H dan daftar B (F0H) mengandungi nilai 4AH. Apakah lokasi dalaman RAM yang berubah dan apakah nilai barunya setelah arahan-arahan berikut terlaksana?

PUSH ACC
PUSH FOH

(4 marks/*markah*)

Q12. Write an 8051 program based on the following sequence of requirements:
Tuliskan satu program 8051 berdasarkan kepada keperluan-keperluan dalam turutan berikut:

i). Clear the accumulator
Bersihkan pengumpuk.

ii). Add the value of 42H to the accumulator.
Tambah nilai 42H kepada pengumpuk berkenaan.

iii). Subtract the value of 82H from the accumulator.
Tolak nilai 82H dari pengumpuk berkenaan.

iv). Add the content of address 64H to the accumulator.
Tambah dengan kandungan alamat 64H kepada pengumpuk tersebut.

v). Compare the result of the accumulator with the contents of memory location 35H. If it is equal, send the value of FFH through Port 2 and end the program. Otherwise, jump to the first instruction.
Bandingkan keputusan pada pengumpuk dengan kandungan alamat 35H. Jika sama nilai, hantarkan nilai FFH melalui Liang 2 dan tamatkan program. Sebaliknya, lompat ke arahan pertama.

(7 marks/*markah*)

Q13. Write a program to add two 4-digit binary-coded decimal numbers. First number is in memory locations of 50H (MSB) and 51H. Second number is in memory locations of 52H (MSB) and 53H. Save the result in memory locations of 50H and 51H.
Tuliskan satu program untuk menambah dua nombor BCD 4 digit. Nombor pertama berada dalam lokasi ingatan 50H (MSB) dan 51H. Nombor kedua berada dalam lokasi ingatan 52H (MSB) dan 53H. Simpan keputusannya dalam lokasi ingatan 50H dan 51H.

(6 marks/*markah*)

Q14. How long does the following TOLAK subroutine to be executed in Program Q14? (Assume 1 machine cycle = 1 μs).
Berapa lamakah untuk subrutin TOLAK dilaksanakan seperti Program Q14? (Anggap 1 kitaran mesin = 1 μs).

```
TOLAK:  MOV   R0,#40H
LOOP:   MOV   @R0,#0
        INC   R0
        CJNE  R0,#60H,LOOP
        RET
```

Program Q14. TOLAK Subroutine / *Subrutin TOLAK*

(6 marks/*markah*)

Q15. Convert the TOLAK subroutine into machine language.
Tukarkan subrutin TOLAK ke dalam bahasa mesin.

(10 marks/*markah*)

Q16. Determine the value for TMOD to use Timer 0 in mode 2, with 8051 XTAL for clock source, and use instructions to start and stop the timer.
Tentukan nilai untuk TMOD bagi penggunaan Pemasa 0 dalam mod 2, dengan XTAL 8051 sebagai sumber jam dan menggunakan arahan-arahan untuk menghidup dan menghentikan pemasa tersebut.

(3 marks/*markah*)

Q17. Write an 8051 program to generate a 100 Hz signal on port P1.0, using timer-0. The signal should have a 50 % duty cycle.
Tuliskan satu program 8051 untuk menjana isyarat 100 Hz pada liang P1.0 menggunakan pemasa-0. Isyarat ini mempunyai kitar kerja 50 %.

(7 marks/*markah*)

Q18. **Program Q18** is a delay subroutine in assembly language. Assuming a 12 MHz oscillator is used. Calculate the delay for the subroutine. Show your calculation to support your answer.

Program Q18 *adalah suatu subrutin lengah dalam bahasa himpunan. Anggap pengayun 12 MHz digunakan. Kirakan lengah masa untuk subrutin ini. Tunjukkan pengiraan anda bagi menyokong jawapan yang diberikan.*

(5 marks/*markah*)

```
DELAY:   MOV   TMOD,#10H
ULANG:   MOV   TH1,#9EH
         MOV   TL1,#58H
         SETB  TR1
LOOP:    JNB   TF1,LOOP
         CLR   TR1
         CLR   TF1
         SJMP  ULANG
         RET
```

Program Q18 Delay Subroutine/ *Subrutin Lengah*

Q19. (a) Write the instructions to enable the serial interrupt, Timer 0 interrupt and external interrupt 1 (INT1).

Tuliskan arahan-arahan untuk menghidupkan sampukan sesiri, sampukan Pemasa 0 dan sampukan luaran 1 (INT1).

(2 marks/*markah*)

(b) The following instruction is executed by an 8051 micro-controller. Discuss the sequence in which the interrupts are serviced.

Arahan berikut dilaksanakan oleh mikropengawal 8051. Bincangkan aturan jujukan di mana sampukan dilayan.

```
MOV   IP,#00001100B
```

(5 marks/*markah*)

Q20. A 4-bit DIP switch and a common-anode 7-segment display are connected to 8051 as shown in **Figure Q20**. Write a program that continually reads a 4-bit code from the DIP switch and updates the segments to display the appropriate hexadecimal character. For example, if the code 1110B is read, the hexadecimal character "E" should appear.

Satu suis DIP 4 bit dan paparan 7-ruas anod sepunya disambungkan kepada 8051 seperti yang ditunjukkan pada ***Rajah Q20****. Tuliskan satu program yang membaca secara berterusan kod 4-bit daripada suis DIP dan mengemaskini paparan pada ruas-ruas untuk memaparkan huruf heksadesimal yang tertentu. Sebagai contoh, jika kod 1110B dibaca, huruf heksadesimal "E" akan muncul.*

(20 marks/*markah*)

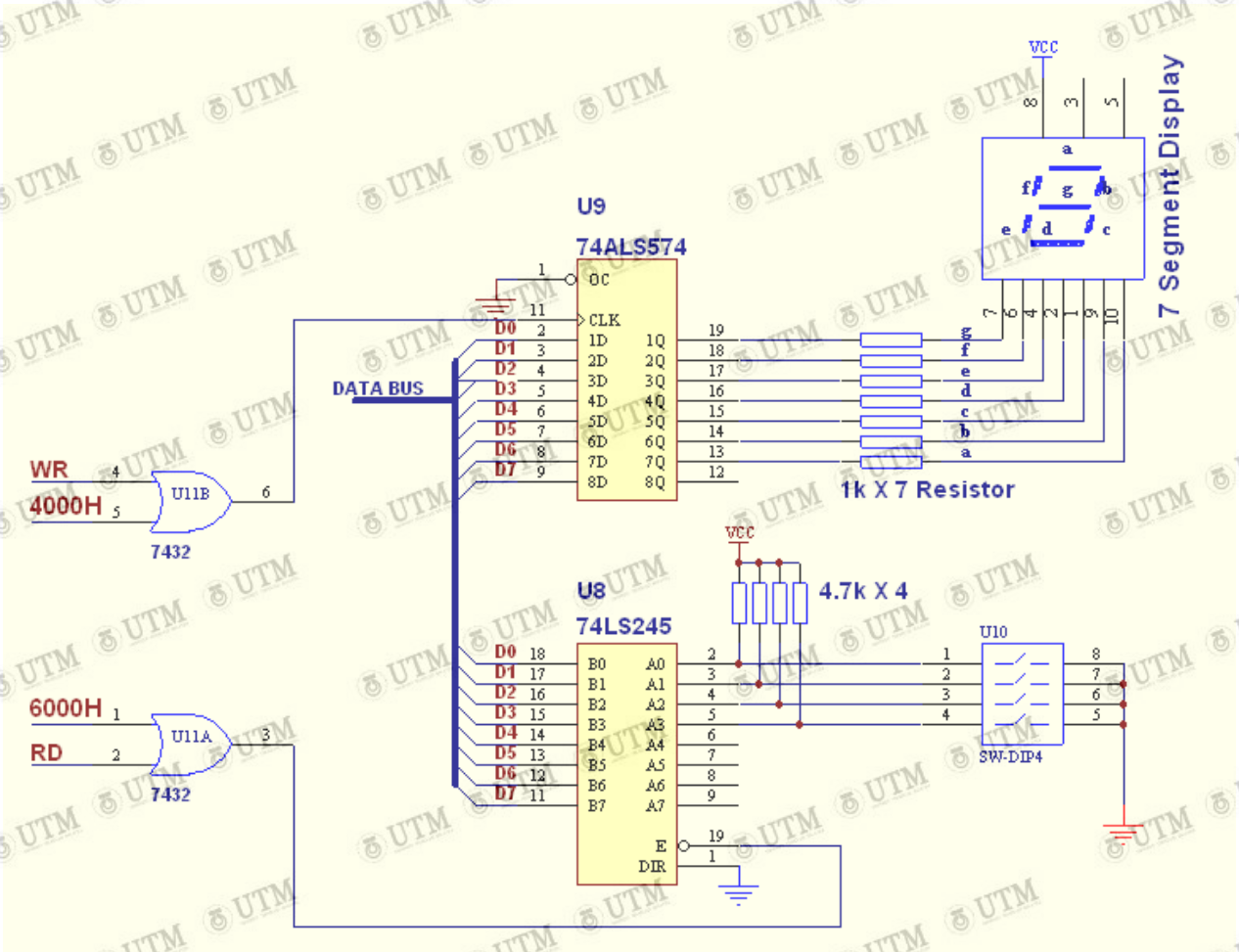
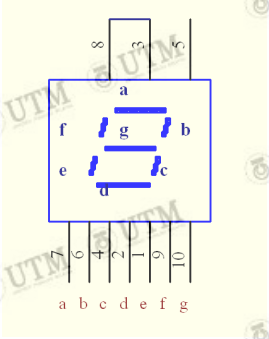


Figure Q20 / ***Rajah Q20***

Seven Segment display lookup tables



Display	Common Anode	Common Cathode
0	C0	3F
1	F9	06
2	A4	5B
3	B0	4F
4	99	66
5	92	6D
6	82	7D
7	F8	07
8	80	7F
9	98	67
A	88	77
C	C6	39
E	86	79
F	8E	71
G	82	70
H	89	76
.	7F	80
Blank	FF	00

Instruction Code Summary

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	JBC bit, rel	JB bit, rel	JNB bit, rel	JC rel	JNC rel	JZ rel	JNZ rel	SJMP rel	MOV DPTR, # data 16	ORL C, /bit	ANL C, /bit	PUSH dir	POP dir	MOVX A, @DPTR	MOVX @DPTR, A
1	AJMP (P0)	ACALL (P0)	AJMP (P1)	ACALL (P1)	AJMP (P2)	ACALL (P2)	AJMP (P3)	ACALL (P3)	AJMP (P4)	ACALL (P4)	AJMP (P5)	ACALL (P5)	AJMP (P6)	ACALL (P6)	AJMP (P7)	ACALL (P7)
2	LJMP addr16	LCALL addr16	RET	RETI	ORL dir, A	ANL dir, A	XRL dir, A	ORL C, bit	ANL C, bit	MOV bit, C	MOV C, bit	CPL bit	CLR bit	SETB bit	MOVX A, @R0	MOVX @R0, A
3	RR A	RRC A	RL A	RLC A	ORL dir, # data	ANL dir, # data	XRL dir, # data	JMP @A+DPTR	MOVC A, @A+PC	MOVC A, @A+DPTR	INC DPTR	CPL C	CLR C	SETB C	MOVX A, @R1	MOVX @R1, A
4	INC A	DEC A	ADD A, # data	ADDC A, # data	ORL A, # data	ANL A, # data	XRL A, # data	MOV A, # data	DIV AB	SUBB A, # data	MUL AB	CJNE A, # data, rel	SWAP A	DA A	CLR A	CPL A
5	INC dir	DEC dir	ADD A, dir	ADDC A, dir	ORL A, dir	ANL A, dir	XRL A, dir	MOV dir, # data	MOV dir, dir	SUBB A, dir		CJNE A, dir, rel	XCH A, dir	DJNZ dir, rel	MOV A, dir	MOV dir, A
6	INC @R0	DEC @R0	ADD A, @R0	ADDC A, @R0	ORL A, @R0	ANL A, @R0	XRL A, @R0	MOV @R0, # data	MOV dir, @R0	SUBB A, @R0	MOV @R0, dir	CJNE @R0, # data, rel	XCH A, @R0	XCHD A, @R0	MOV A, @R0	MOV @ R0, A
7	INC @R1	DEC @R1	ADD A, @R1	ADDC A, @R1	ORL A, @R1	ANL A, @R1	XRL A, @R1	MOV @R1, # data	MOV dir, @R1	SUBB A, @R1	MOV @R1, dir	CJNE @R1, # data, rel	XCH A, @R1	XCHD A, @R1	MOV A, @R1	MOV @ R1, A
8	INC R0	DEC R0	ADD A, R0	ADDC A, R0	ORL A, R0	ANL A, R0	XRL A, R0	MOV R0, # data	MOV dir, R0	SUBB A, R0	MOV R0, dir	CJNE R0, # data, rel	XCH A, R0	DJNZ R0, rel	MOV A, R0	MOV R0, A
9	INC R1	DEC R1	ADD A, R1	ADDC A, R1	ORL A, R1	ANL A, R1	XRL A, R1	MOV R1, # data	MOV dir, R1	SUBB A, R1	MOV R1, dir	CJNE R1, # data, rel	XCH A, R1	DJNZ R1, rel	MOV A, R1	MOV R1, A
A	INC R2	DEC R2	ADD A, R2	ADDC A, R2	ORL A, R2	ANL A, R2	XRL A, R2	MOV R2, # data	MOV dir, R2	SUBB A, R2	MOV R2, dir	CJNE R2, # data, rel	XCH A, R2	DJNZ R2, rel	MOV A, R2	MOV R2, A
B	INC R3	DEC R3	ADD A, R3	ADDC A, R3	ORL A, R3	ANL A, R3	XRL A, R3	MOV R3, # data	MOV dir, R3	SUBB A, R3	MOV R3, dir	CJNE R3, # data, rel	XCH A, R3	DJNZ R3, rel	MOV A, R3	MOV R3, A
C	INC R4	DEC R4	ADD A, R4	ADDC A, R4	ORL A, R4	ANL A, R4	XRL A, R4	MOV R4, # data	MOV dir, R4	SUBB A, R4	MOV R4, dir	CJNE R4, # data, rel	XCH A, R4	DJNZ R4, rel	MOV A, R4	MOV R4, A
D	INC R5	DEC R5	ADD A, R5	ADDC A, R5	ORL A, R5	ANL A, R5	XRL A, R5	MOV R5, # data	MOV dir, R5	SUBB A, R5	MOV R5, dir	CJNE R5, # data, rel	XCH A, R5	DJNZ R5, rel	MOV A, R5	MOV R5, A
E	INC R6	DEC R6	ADD A, R6	ADDC A, R6	ORL A, R6	ANL A, R6	XRL A, R6	MOV R6, # data	MOV dir, R6	SUBB A, R6	MOV R6, dir	CJNE R6, # data, rel	XCH A, R6	DJNZ R6, rel	MOV A, R6	MOV R6, A
F	INC R7	DEC R7	ADD A, R7	ADDC A, R7	ORL A, R7	ANL A, R7	XRL A, R7	MOV R7, # data	MOV dir, R7	SUBB A, R7	MOV R7, dir	CJNE R7, # data, rel	XCH A, R7	DJNZ R7, rel	MOV A, R7	MOV R7, A

2Byte	3Byte
2Cycle	4Cycle

The Program Status Word (PSW)

Bit	Symbol	Address	Description
PSW.7	CY	D7H	Carry flag
PSW.6	AC	D6H	Auxiliary carry flag
PSW.5	F0	D5H	Flag 0
PSW.4	RS1	D4H	Register bank select 1
PSW.3	RS0	D3H	Register bank select 0
PSW.2	OV	D2H	Overflow flag
PSW.1	--	D1H	Reserved
PSW.0	P	D0H	Parity Flag.

RS1	RS0	Bank	Address
0	0	0	00H – 07H
0	1	1	08H – 1FH
1	0	2	10H – 17H
1	1	3	18H – 1FH

Timer Mode (TMOD) register summary

Bit	Name	Timer	Description
7	GATE	1	When this bit is set the timer will only run when INT1(P3.3) is high(hardware control). When this bit is cleared the timer will run regardless of the state of INT1(software control.
6	C/T	1	Counter/timer select bit. 1 = counter operation 0 = timer operation
5	M1	1	Mode bit 1
4	M0	1	Mode bit 0
3	GATE	0	Timer 0 gate bit
2	C/T	0	Timer 0 counter/timer select bit
1	M1	0	Timer 0 M1 bit
0	M0	0	Timer 0 M0 bit

M1	M0	Mode	Description
0	0	0	13-bit timer mode (8048 mode)
0	1	1	16-bit timer mode

1	0	2	8-bit auto-reload mode
1	1	3	Split timer mode Timer 0: TL0 is an 8-bit timer controlled by timer 0 mode bits; TH0, the same except controlled by timer 1 mode bits Timer1: stopped

Timer Control (TCON) register summary

Bit	SYMBOL	BIT ADDRESS	DESCRIPTION
TCON.7	TF1	8FH	Timer 1 overflow flag. Set by hardware upon overflow; cleared by software, or by hardware when processor vectors to interrupt service routine
TCON.6	TR1	8EH	Timer 1 run-control bit. Set/cleared by software to turn timer on/off
TCON.5	TF0	8DH	Timer 0 overflow bit. Do the same function as TF1 but for Timer 0
TCON.4	TR0	8CH	Timer 0 run-control bit. Do the same function as TR1 but for Timer 0
TCON.3	IE1	8BH	External interrupt 1 edge flag. Set by hardware when a falling edge is detected on INT1;cleared by software, or by hardware when CPU vectors to interrupt service routine
TCON.2	IT1	8AH	External interrupt 1 type flag. Set/cleared by software for falling edge/low-level activated external interrupt.
TCON.1	IE0	89H	External interrupt 0 edge flag. Do the same function as IE1 but for external interrupt-0.
TCON.0	IT0	88H	External interrupt 0 type flag. Do the same function as IT1 but for external interrupt-0.

Table 6-1 Interrupt Enable (IE) register summary

Bit	Symbol	Bit Address	Description (1 = enable, 0 = disable)
IE.7	EA	AFH	Global enable/disable. EA = 1, each individual source is enabled/disabled by setting/clearing its enable bit. EA= 0, disable all interrupts.
IE.6	-	AEH	Undefined
IE.5	ET2	ADH	Enable Timer 2 interrupt(8052)
IE.4	ES	ACH	Enable serial port interrupt
IE.3	ET1	ABH	Enable Timer 1 interrupt
IE.2	EX1	AAH	Enable external 1 interrupt
IE.1	ET0	A9H	Enable Timer 0 interrupt
IE.0	EX0	A8H	Enable external 0 interrupt

Interrupt Priority (IP) Register

Bit	Symbol	Bit Address	Description (1 = Higher level, 0 = lower level)
IP.7	-	-	Undefined
IP.6	-	-	Undefined
IP.5	PT2	BDH	Priority for Timer 2 interrupt(8052)
IP.4	PS	BCH	Priority for serial port interrupt
IP.3	PT1	BBH	Priority for Timer 1 interrupt
IP.2	PX1	BAH	Priority for external 1 interrupt
IP.1	PT0	B9H	Priority for Timer 0 interrupt
IP.0	PX0	B8H	Priority for external 0 interrupt

Interrupt Vectors

Interrupt	Flag	Bit Address
System Reset	RST	0000H
External 0	IE0	0003H
Timer 0	TF0	000BH

External 1	IE1	0013H
Timer 1	TF1	001BH
Serial Port	RI or TI	0023H
Timer 2	TF2 or EXF2	002BH

Register values after system reset(power-up)

REGISTER(S)	**CONTENTS**
Program Counter	0000H
Accumulator	00H
B register	00H
PSW	00H
SP	07H
DPTR	0000H
Ports 0 – 3	FFH
IP	XXX00000B
Timer Register	00H
SCON	00H
SBUF	00H
PCON(HMOS)	0XXXXXXXB
PCON(CMOS)	0XXX0000B